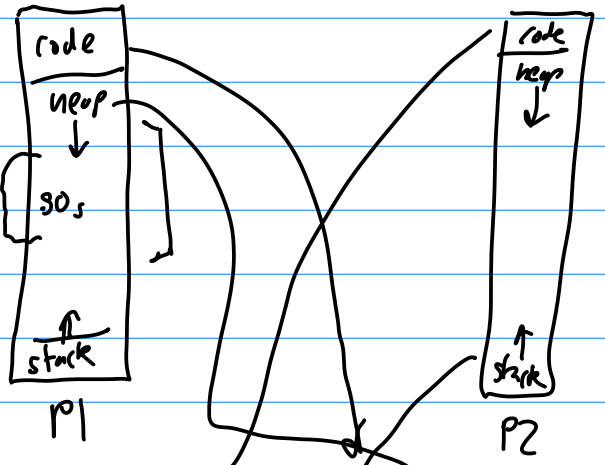
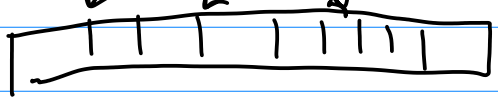
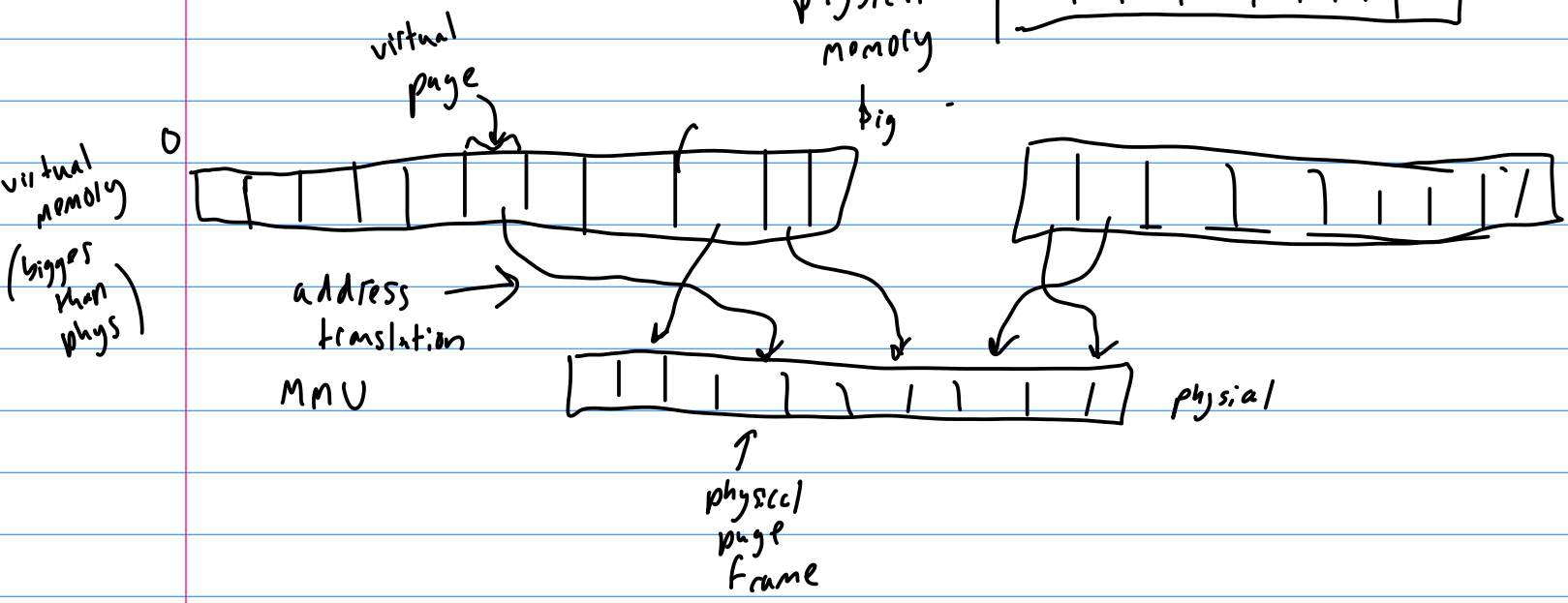
CS 3214 lecture # 21 "virtual memory"

Memory management
heap - explict/manual
automatic





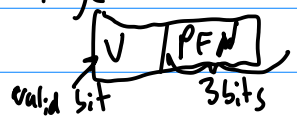


Address translation virt address → physical address

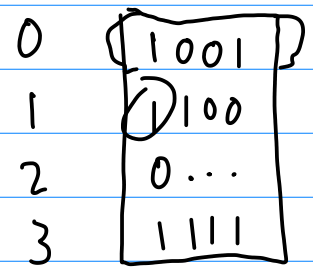
MMU

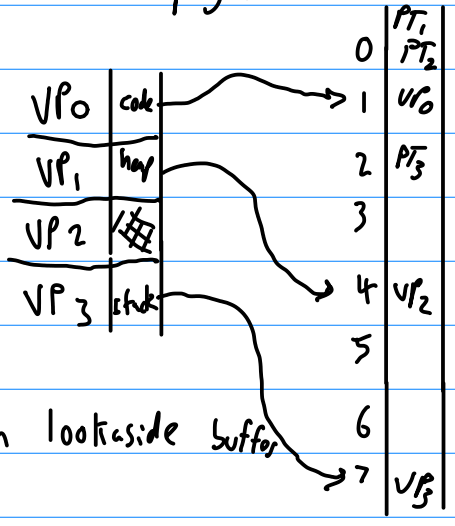
PTBR register

Page table



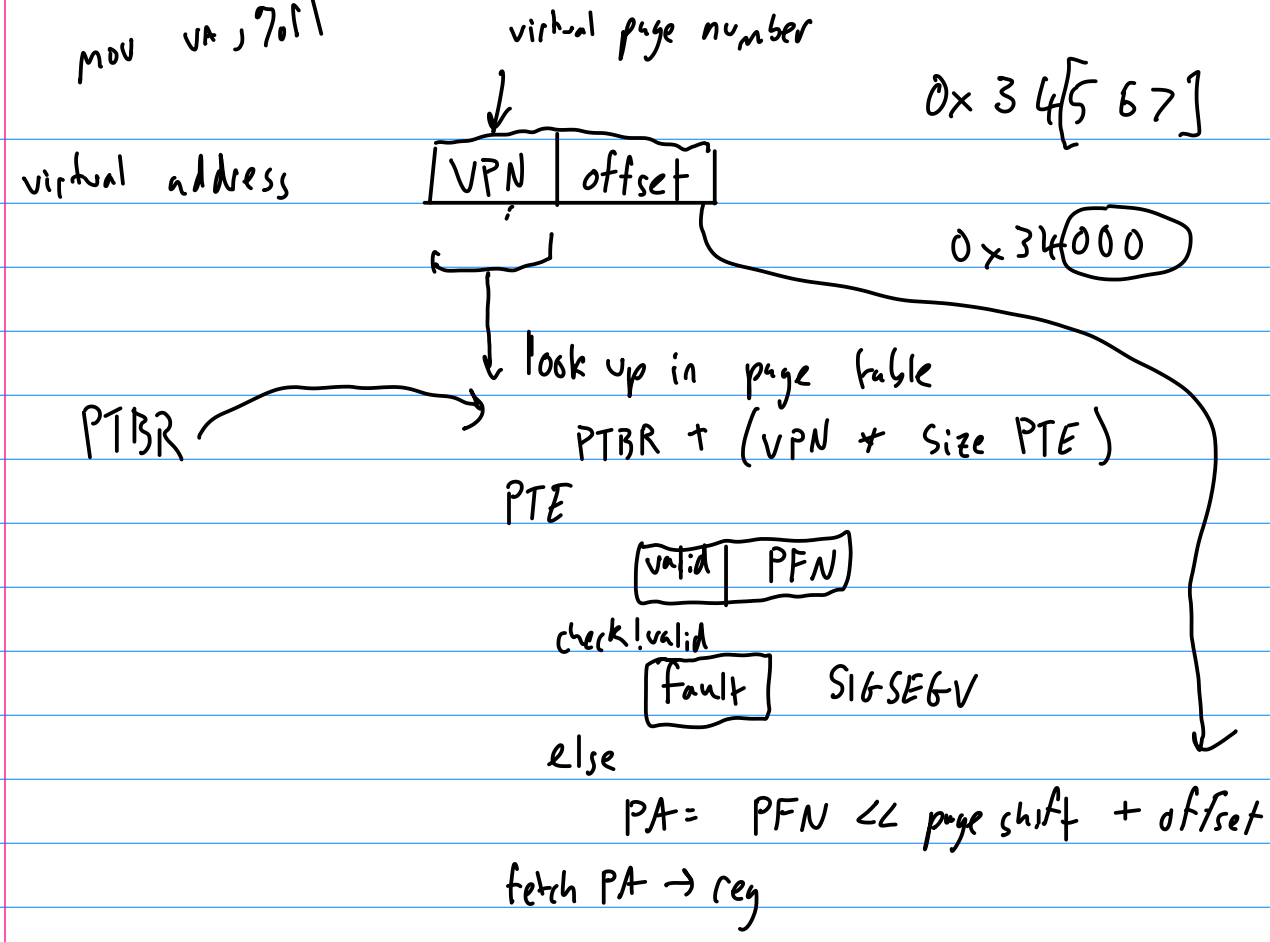
PTE





TLB - translation lookaside buffer

mov va, %ax

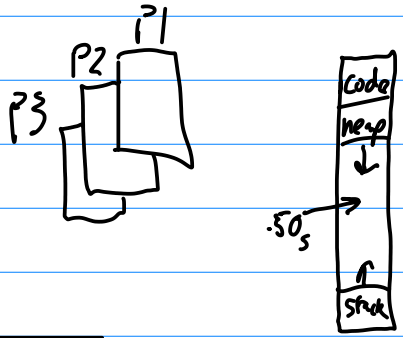


PTE : mapping
valid
asid
permissions (r,w,x) e.g.
granularity for permissions

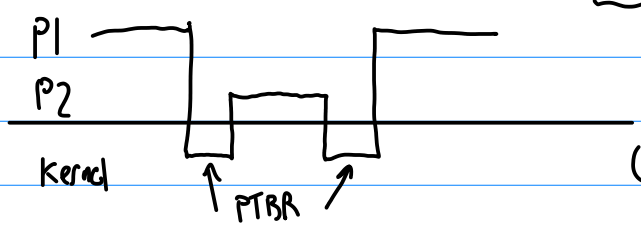
TLB

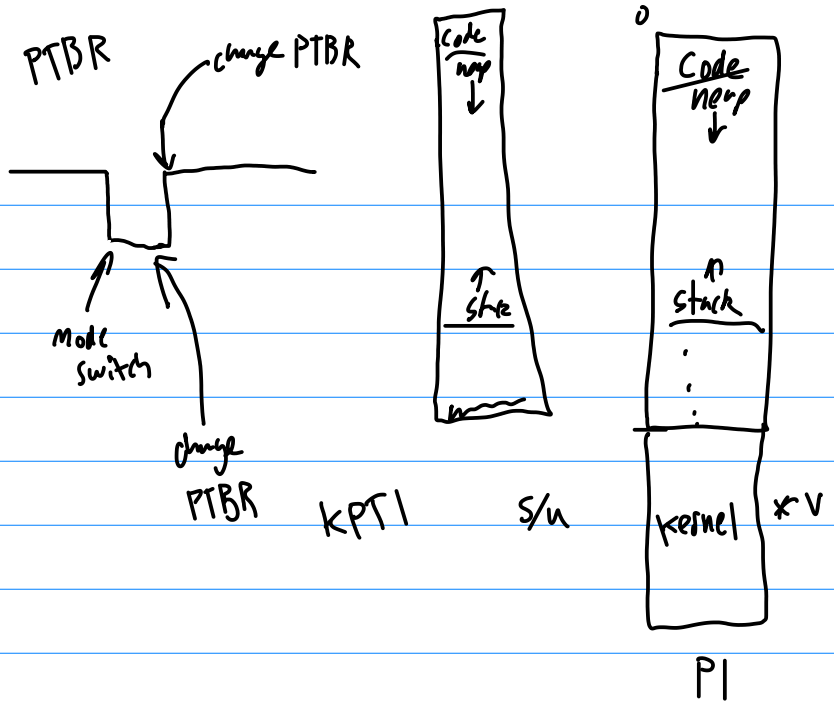
big pages ?
+ faster (better TLB coverage)
- waste of space
+ less space for page tables

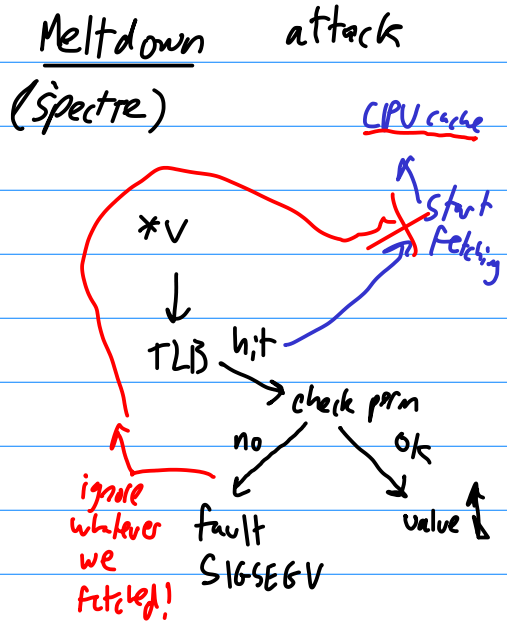
Virtual Memory : goals
- private address spaces
- more memory than phys. machine
- protection - processes
  - kernel



Context switch







Intel MPK
memory protection keys

Next time: what address space looks like
where memory actually lives
demand paging