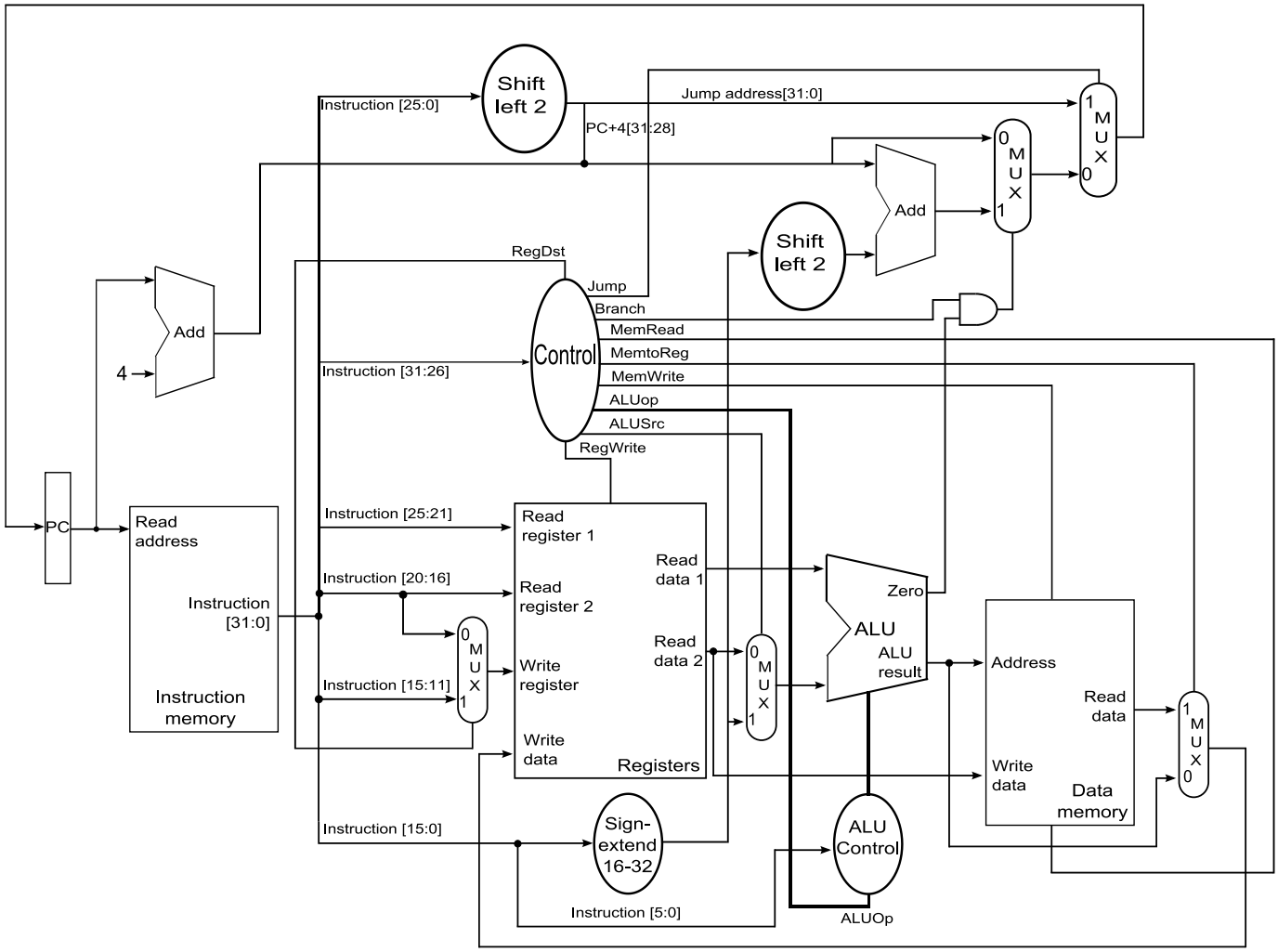
The single-cycle MIPS32 datapath:



Supported instructions: add, sub, and, or, slt, lw, sw, beq, j

Specifications of supported MIPS assembly instructions:

```
add  $rd, $rs, $rt          # GPR[rd] = GPR[rs] + GPR[rt]
sub  $rd, $rs, $rt          # GPR[rd] = GPR[rs] - GPR[rt]
and  $rd, $rs, $rt          # GPR[rd] = GPR[rs] & GPR[rt]
or   $rd, $rs, $rt          # GPR[rd] = GPR[rs] | GPR[rt]
slt  $rd, $rs, $rt          # GPR[rd] = GPR[rs] < GPR[rt] ? 1 : 0
lw   $rt, imm16($rs)        # GPR[rt] = Mem[ GPR[rs] + imm16 ]
sw   $rt, imm16($rs)        # Mem[ GPR[rs] + imm16 ] = GPR[rt]
beq  $rs, $rt, offset       # PC <-- (rs == rt ? PC + 4 + offset << 2)
                            #                  : PC + 4)
j    target                 # PC <-- ( (PC+4)(31:28) || (target << 2))
```

The preliminary pipelined MIPS32 datapath with interstage buffers for synchronization: