Operation	Time to Stabilize
Register Read/Write	100 ps
ALU/Adder operation	200 ps
Memory Read/Write	200 ps
Sign-Extension	50 ps

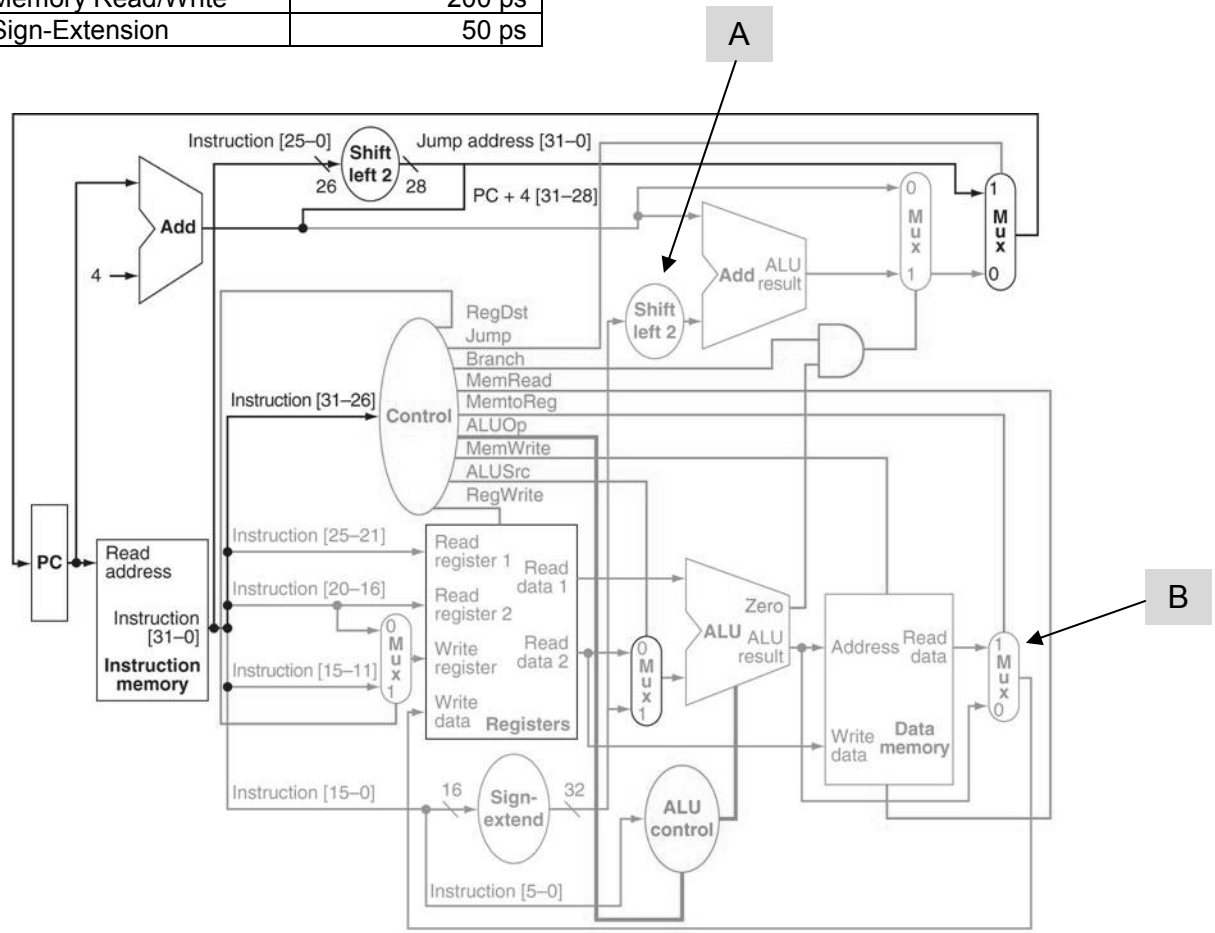

Figure 4.24

The single-cycle MIPS datapath for the instructions `add`, `sub`, `and`, `or`, `slt`, `lw`, `sw`, `beq` and `j`.

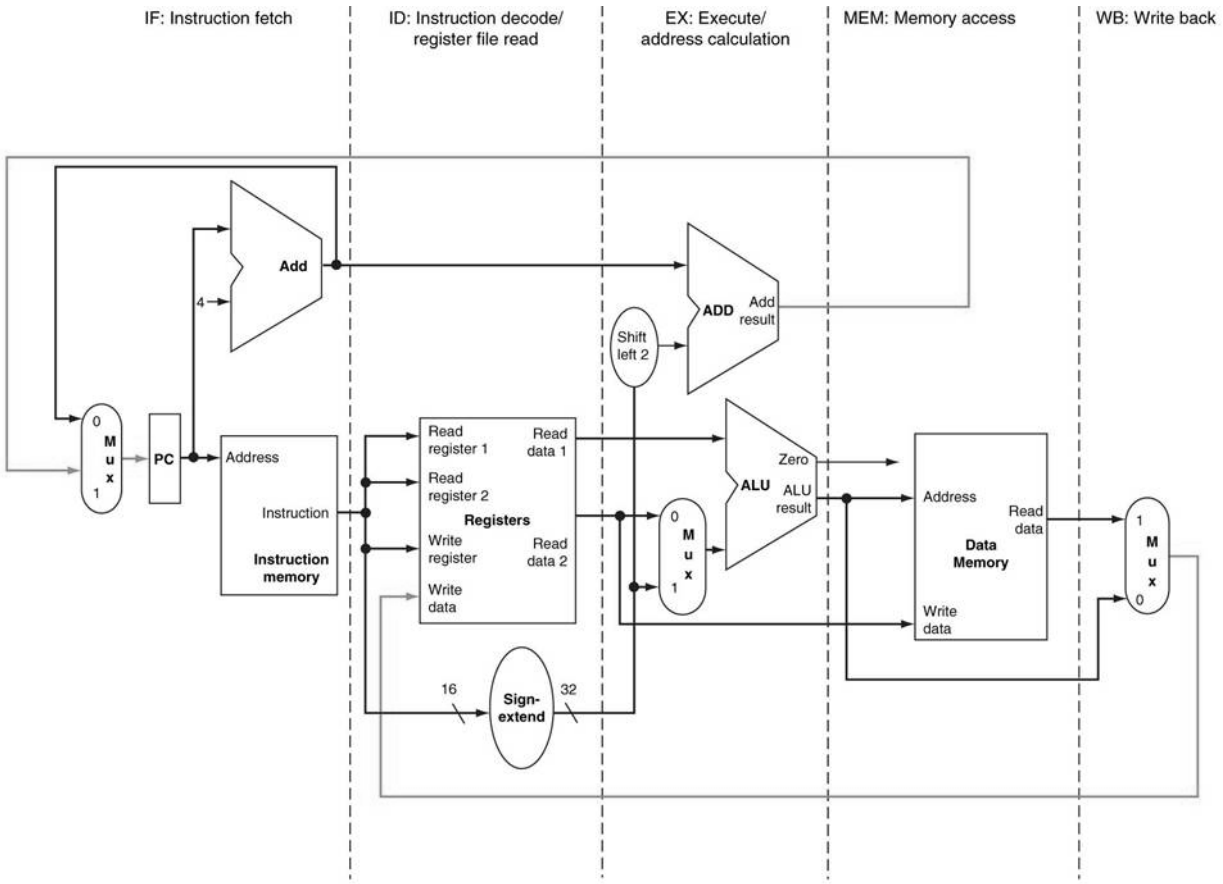

Figure 4.33

The stages for the single-cycle MIPS pipeline for the instructions `add`, `sub`, `and`, `or`, `slt`, `lw`, `sw`, and `beq`.