Router Architecture Overview

Two key router functions:

- run routing algorithms/protocol (RIP, OSPF, BGP)
- *switching* datagrams from incoming to outgoing link
Input Port Functions

Decentralized switching:
- given datagram dest., lookup output port using routing table in input port memory
- goal: complete input port processing at ‘line speed’
- queuing: if datagrams arrive faster than forwarding rate into switch fabric

Physical layer:
- bit-level reception

Data link layer:
Input Port Queuing

- Fabric slower than input ports combined -> queuing may occur at input queues
- **Head-of-the-Line (HOL) blocking**: queued datagram at front of queue prevents others in queue from moving forward
- *queuing delay and loss due to input buffer overflow!*

![Diagram showing input port queuing and HOL blocking](image)
Three types of switching fabrics

- **Memory**
- **Bus**
- **Crossbar**
Switching Via Memory

First generation routers:
• packet copied by system’s (single) CPU
• speed limited by memory bandwidth (2 bus crossings per datagram)

Modern routers:
• input port processor performs lookup, copy into memory
• Cisco Catalyst 8500
Switching Via Bus

- datagram from input port memory
to output port memory via a shared bus
- **bus contention:** switching speed limited by bus bandwidth
- 1 Gbps bus, Cisco 1900: sufficient speed for access and enterprise routers (not regional or backbone)
Switching Via An Interconnection Network

- overcome bus bandwidth limitations
- Banyan networks, other interconnection nets initially developed to connect processors in multiprocessor
- Advanced design: fragmenting datagram into fixed length cells, switch cells through the fabric.
- Cisco 12000: switches Gbps through the interconnection network
• **Buffering** required when datagrams arrive from fabric faster than the transmission rate
• **Scheduling discipline** chooses among queued datagrams for transmission
Output port queuing

- buffering when arrival rate via switch exceeds output line speed
- *queuing (delay) and loss due to output port buffer overflow!*
IPv6

- **Initial motivation:** 32-bit address space completely allocated by 2008.
- **Additional motivation:**
  - header format helps speed processing/forwarding
  - header changes to facilitate QoS
  - new “anycast” address: route to “best” of several replicated servers
IP Version 6

- **Features**
  - 128-bit addresses (classless)
  - multicast
  - real-time service
  - authentication and security
  - autoconfiguration
  - end-to-end fragmentation
  - protocol extensions

- **Header**
  - 40-byte “base” header
  - extension headers (fixed order, mostly fixed length)
    - fragmentation
    - source routing
    - authentication and security
    - other options
IPv6 Header (Cont)

**Priority:** identify priority among datagrams in flow

**Flow Label:** identify datagrams in same “flow.”
(concept of “flow” not well defined).

**Next header:** identify upper layer protocol for data

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<thead>
<tr>
<th>ver</th>
<th>pri</th>
<th>flow label</th>
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<td>destination address (128 bits)</td>
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<td>data</td>
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32 bits
Other Changes from IPv4

- **Checksum**: removed entirely to reduce processing time at each hop
- **Options**: allowed, but outside of header, indicated by “Next Header” field
- **ICMPv6**: new version of ICMP
  - additional message types, e.g. “Packet Too Big”
  - multicast group management functions
Transition From IPv4 To IPv6

- Not all routers can be upgraded simultaneously
  - no “flag days”
  - How will the network operate with mixed IPv4 and IPv6 routers?

- Two proposed approaches:
  - *Dual Stack*: some routers with dual stack (v6, v4) can “translate” between formats
  - *Tunneling*: IPv6 carried as payload n IPv4 datagram among IPv4 routers
Dual Stack Approach
Tunneling

IPv6 inside IPv4 where needed