

4.36 [15] <§§2.3, 4.11> Using Figure 4.54 on page 311, calculate the average clock cycles per instruction (CPI) for the program gcc. Figure 4.55 gives the average CPI per instruction category, taking into account cache misses and other effects. Assume that instructions omitted from the table have a CPI of 1.0.

Instruction category	Average CPI
Loads and stores	1.4
Conditional branch	1.8
Jumps	1.2
Integer multiply	10.0
Integer divide	30.0
Floating-point add and subtract	2.0
Floating-point multiply, single precision	4.0
Floating-point multiply, double precision	5.0
Floating-point divide, single precision	12.0
Floating-point divide, double precision	19.0

FIGURE 4.55 CPI for MIPS instruction categories.

4.37 [15] <§§2.3, 4.11> This exercise is similar to Exercise 4.36, but this time replace the program gcc with the program spice.

4.38 [2 weeks] Write a simulator for a subset of the MIPS instruction set using MIPS instructions and the SPIM simulator described in Appendix A. Your simulator should execute hand-assembled programs that are located in the data segment of the SPIM simulator and should use \$v0 and \$v1 for input and output. Other portions of the data segment can be used for storing the memory contents and register values of your virtual machine. Your implementation can use any of the MIPS instructions, but your simulator need only support a smaller subset of the instruction set (e.g., the instructions appearing in Chapters 5 and 6). (Additional details regarding this assignment are available at www.mkp.com/cod2e.htm.)

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4.39 [1 week] {Ex. 4.38} Add an exception handler to the simulator you developed for Exercise 4.38. Your simulator should generate a simulated exception if a misaligned word is accessed via an lw, sw, or jr instruction. The exception handler should print out an error message identifying the offending address (within the simulation) and then realign the access, perform the instruction, and resume executing the simulated program. (Additional details regarding this assignment are available at www.mkp.com/cod2e.htm.)

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