

## KVR400X64C3AK2/1G 1GB (512MB 64M x 64-Bit x 2 pcs.) DDR400 CL3 184-Pin DIMM Kit

### DESCRIPTION

ValueRAM's KVR400X64C3AK2/1G is a kit of two 64M x 64-bit (512MB) DDR400 CL3 SDRAM (Synchronous **DRAM**) memory modules. Total kit capacity is 1GB (1024MB). The components on each module include sixteen 32M x 8-bit (8M x 8-bit x 4 Bank) DDR400 SDRAM in TSOP packages. Each 184-pin DIMM uses gold contact fingers and requires +2.6V. The electrical and mechanical specifications are as follows:

### FEATURE

- Power supply : Vdd: 2.6V ± 0.1V, Vddq: 2.6V ± 0.1V
- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional data strobe(DQS)
- Differential clock inputs(CK and  $\overline{CK}$ )
- DLL aligns DQ and DQS transition with CK transition
- Programmable Read latency 3 (clock)
- Programmable Burst length (2, 4, 8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input
- Auto & Self refresh, 7.8us refresh interval(8K/64ms refresh)
- Serial presence detect with EEPROM
- PCB : Height 1.250" (31.75mm), double sided component

### PIN CONFIGURATIONS (Front side/back side)

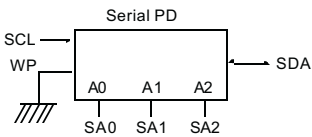
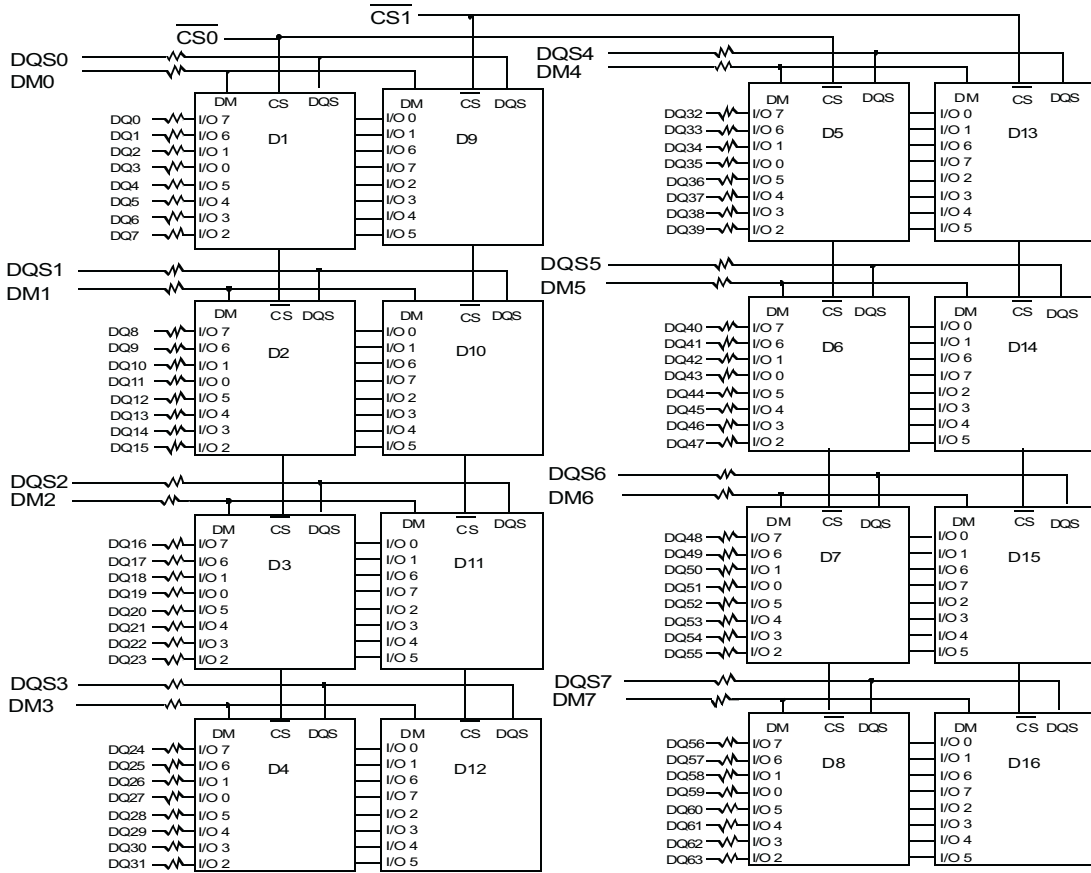
Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VREF	32	A5	62	VDDQ	93	VSS	124	VSS	154	/RAS
2	DQ0	33	DQ24	63	/WE	94	DQ4	125	A6	155	DQ45
3	VSS	34	VSS	64	DQ41	95	DQ5	126	DQ28	156	VDDQ
4	DQ1	35	DQ25	65	/CAS	96	VDDQ	127	DQ29	157	/CS0
5	DQS0	36	DQS3	66	VSS	97	DM0	128	VDDQ	158	/CS1
6	DQ2	37	A4	67	DQS5	98	DQ6	129	DM3	159	DM5
7	VDD	38	VDD	68	DQ42	99	DQ7	130	A3	160	VSS
8	DQ3	39	DQ26	69	DQ43	100	VSS	131	DQ30	161	DQ46
9	NC	40	DQ27	70	VDD	101	NC	132	VSS	162	DQ47
10	NC	41	A2	71	*/CS2	102	NC	133	DQ31	163	*/CS3
11	VSS	42	VSS	72	DQ48	103	NC	134	*CB4	164	VDDQ
12	DQ8	43	A1	73	DQ49	104	VDDQ	135	*CB5	165	DQ52
13	DQ9	44	*CB0	74	VSS	105	DQ12	136	VDDQ	166	DQ53
14	DQS1	45	*CB1	75	/CK2	106	DQ13	137	CK0	167	*A13
15	VDDQ	46	VDD	76	CK2	107	DM1	138	/CK0	168	VDD
16	CK1	47	*DQS8	77	VDDQ	108	VDD	139	VSS	169	DM6
17	/CK1	48	A0	78	DQS6	109	DQ14	140	*DM8	170	DQ54
18	VSS	49	*CB2	79	DQ50	110	DQ15	141	A10	171	DQ55
19	DQ10	50	VSS	80	DQ51	111	CKE1	142	*CB6	172	VDDQ
20	DQ11	51	*CB3	81	VSS	112	VDDQ	143	VDDQ	173	NC
21	CKE0	52	BA1	82	VDDID	113	*BA2	144	*CB7	174	DQ60
22	VDDQ	KEY		83	DQ56	114	DQ20	KEY		175	DQ61
23	DQ16	53	DQ32	84	DQ57	115	A12	145	VSS	176	VSS
24	DQ17	54	VDDQ	85	VDD	116	VSS	146	DQ36	177	DM7
25	DQS2	55	DQ33	86	DQ57	117	DQ21	147	DQ37	178	DQ62
26	VSS	56	DQS4	87	DQ58	118	A11	148	VDD	179	DQ63
27	A9	57	DQ34	88	DQ59	119	DM2	149	DM4	180	VDDQ
28	DQ18	58	VSS	89	VSS	120	VDD	150	DQ38	181	SA0
29	A7	59	BA0	90	NC	121	DQ22	151	DQ39	182	SA1
30	VDDQ	60	DQ35	91	SDA	122	A8	152	VSS	183	SA2
31	DQ19	61	DQ40	92	SCL	123	DQ23	153	DQ44	184	VDDSPD

### PIN DESCRIPTION

Pin Name	Function
A0 ~ A12	Address input (Multiplexed)
BA0 ~ BA1	Bank Select Address
DQ0 ~ DQ63	Data input/output
DQS0 ~ DQS7	Data Strobe input/output
CK0, CK0 ~ CK2, CK2	Clock input
CKE0, CKE1	Clock enable input
CS0, CS1	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DM0 ~ 7	Data - in mask
VDD	Power supply (2.5V)
VDDQ	Power Supply for DQS(2.5V)
VSS	Ground
VREF	Power supply for reference
VDDSPD	Serial EEPROM Power Supply (2.3V to 3.6V)
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
VDDID	VDD identification flag
NC	No connection

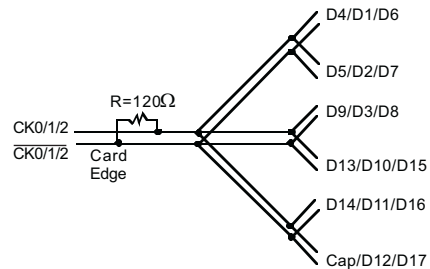
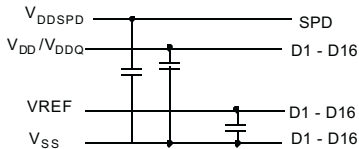
\* These pins are not used in this module.

Functional Block Diagram



Clock Input	SDRAMs
CK0/CK0	4 SDRAMs
CK1/CK1	6 SDRAMs
CK2/CK2	6 SDRAMs

- BA0 - BA1 → BA0-BA1: SDRAMs D1 - D16
- A0 - A12 → A0-An: SDRAMs D1 - D16
- RAS → RAS: SDRAMs D1 - D16
- CAS → CAS: SDRAMs D1 - D16
- V<sub>DDSPD</sub> → SPD
- V<sub>DD</sub>/V<sub>DDQ</sub> → D1 - D16
- VREF → D1 - D16
- V<sub>SS</sub> → D1 - D16
- CKE1 → CKE: 8 SDRAMs
- CKE0 → CKE: 8 SDRAMs
- WE → WE: 16 SDRAMs



- Notes:
1. DQ-to-I/O wiring is shown as recommended but may be changed.
  2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
  3. DQ, DQS, DM resistors: 22 Ohms ± 5%.
  4. BAx, Ax, RAS, CAS, WE resistors: 3 Ohms ± 5%.

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Value	Unit
Input, Output Voltage	V <sub>IN</sub> , V <sub>OUT</sub>	-0.3 ~ V <sub>DDQ</sub> +0.3	V
Power Supply Voltage	V <sub>DD</sub> , V <sub>DDQ</sub>	-0.3 ~ 3.6	V
Operating temperature	T <sub>OPR</sub>	0 ~ 70	°C
Storage temperature	T <sub>STG</sub>	-55 ~ +150	°C
Soldering Temperature	T <sub>SOLDER</sub>	260	V
Power dissipation for each component	P <sub>D</sub>	16	W
Short circuit output current	I <sub>OS</sub>	50	mA

**Note :** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to recommended operating condition. Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

**POWER & DC OPERATING CONDITIONS (SSTL\_2 In/Out)**

Recommended operating conditions(Voltage referenced to V<sub>SS</sub>=0V, T<sub>A</sub>=0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage(for device with a nominal V <sub>DD</sub> of 2.5V)	V <sub>DD</sub>	2.6	2.8		
I/O Supply voltage	V <sub>DDQ</sub>	2.6	V <sub>DD</sub>	V	
I/O Reference voltage	V <sub>REF</sub>	0.49 x V <sub>DDQ</sub>	0.51 x V <sub>DDQ</sub>	V	1
I/O Termination voltage(system)	V <sub>TT</sub>	V <sub>REF</sub> -0.04	V <sub>REF</sub> +0.04	V	2
Input logic high voltage (DC)	V <sub>IH</sub> (DC)	V <sub>REF</sub> +0.15	V <sub>DDQ</sub> +0.3	V	4
Input logic low voltage (DC)	V <sub>IL</sub> (DC)	-0.3	V <sub>REF</sub> -0.15	V	4
Differential Clock DC Input Voltage	V <sub>ICK</sub> (DC)	-0.1	V <sub>DDQ</sub> + 0.1	V	
Input Differential Voltage, CK and $\overline{\text{CK}}$ inputs (DC)	V <sub>ID</sub> (DC)	0.36	V <sub>DDQ</sub> +0.6	V	3
Input high voltage (AC)	V <sub>IH</sub> (AC)	V <sub>REF</sub> +0.31	—	V	
Input high voltage (AC)	V <sub>IL</sub> (AC)		V <sub>REF</sub> -0.31	V	
Input Differential Voltage, CK and $\overline{\text{CK}}$ inputs	V <sub>ID</sub> (AC)	0.7	V <sub>DDQ</sub> + 0.6	V	
Differential AC Input Cross Point Voltage	V <sub>X</sub> (AC)	V <sub>DDQ</sub> /2 - 0.2	V <sub>DDQ</sub> /2 + 0.2	V	
Differential Clock AC Middle	V <sub>ISO</sub> (AC)	V <sub>DDQ</sub> /2 - 0.2	V <sub>DDQ</sub> /2 + 0.2	V	

- Notes**
- Includes  $\pm 25\text{mV}$  margin for DC offset on V<sub>REF</sub>, and a combined total of  $\pm 50\text{mV}$  margin for all AC noise and DC offset on V<sub>REF</sub>, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on V<sub>REF</sub> and internal DRAM noise coupled TO V<sub>REF</sub>, both of which may result in V<sub>REF</sub> noise. V<sub>REF</sub> should be de-coupled with an inductance of  $\leq 3\text{nH}$ .
  - V<sub>TT</sub> is not applied directly to the device. V<sub>TT</sub> is a system supply for signal termination resistors, is expected to be set equal to V<sub>REF</sub>, and must track variations in the DC level of V<sub>REF</sub>
  - V<sub>ID</sub> is the magnitude of the difference between the input level on CK and the input level on  $\overline{\text{CK}}$ .
  - These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a V<sub>REF</sub> envelop that has been bandwidth limited to 200MHZ.
  - The value of V<sub>X</sub> is expected to equal  $0.5 \times V_{DDQ}$  of the transmitting device and must track variations in the dc level of the same.
  - These characteristics obey the SSTL-2 class II standards.

**DDR SDRAM IDD spec table**

Symbol	DDR400 CL3		Unit	Notes
IDD0	1440		mA	
IDD1	1640		mA	
IDD2P	65		mA	
IDD2F	480		mA	
IDD2Q	400		mA	
IDD3P	880		mA	
IDD3N	1200		mA	
IDD4R	2080		mA	
IDD4W	2120		mA	
IDD5	2040		mA	
IDD6	Normal	48	mA	
IDD7A	3080		mA	

\* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

**AC OPERATING CONDITIONS**

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input High Voltage (AC)	$V_{IH} (AC)$	$V_{REF}+0.31$	—	V	3
Input Low Voltage (AC)	$V_{IL} (AC)$		$V_{REF} -0.31$	V	3
Input Differential Voltage, CK and $\overline{CK}$ inputs	$V_{ID} (AC)$	0.7	$V_{DDQ} + 0.6$	V	1
Differential AC Input Cross Point Voltage	$V_X (AC)$	$V_{DDQ}/2 - 0.2$	$V_{DDQ}/2 + 0.2$	V	2
Differential Clock AC Middle	$V_{ISO} (AC)$	$V_{DDQ}/2 - 0.2$	$V_{DDQ}/2 + 0.2$	V	

Note 1. VID is the magnitude of the difference between the input level on CK and the input on  $\overline{CK}$ .

2. The value of  $V_{IX}$  is expected to equal  $0.5 \cdot V_{DDQ}$  of the transmitting device and must track variations in the DC level of the same.

3. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. the AC and DC input specifications are relation to a Vref envelope that has been bandwidth limited 20MHz.

## AC Timing Parameters and Specifications

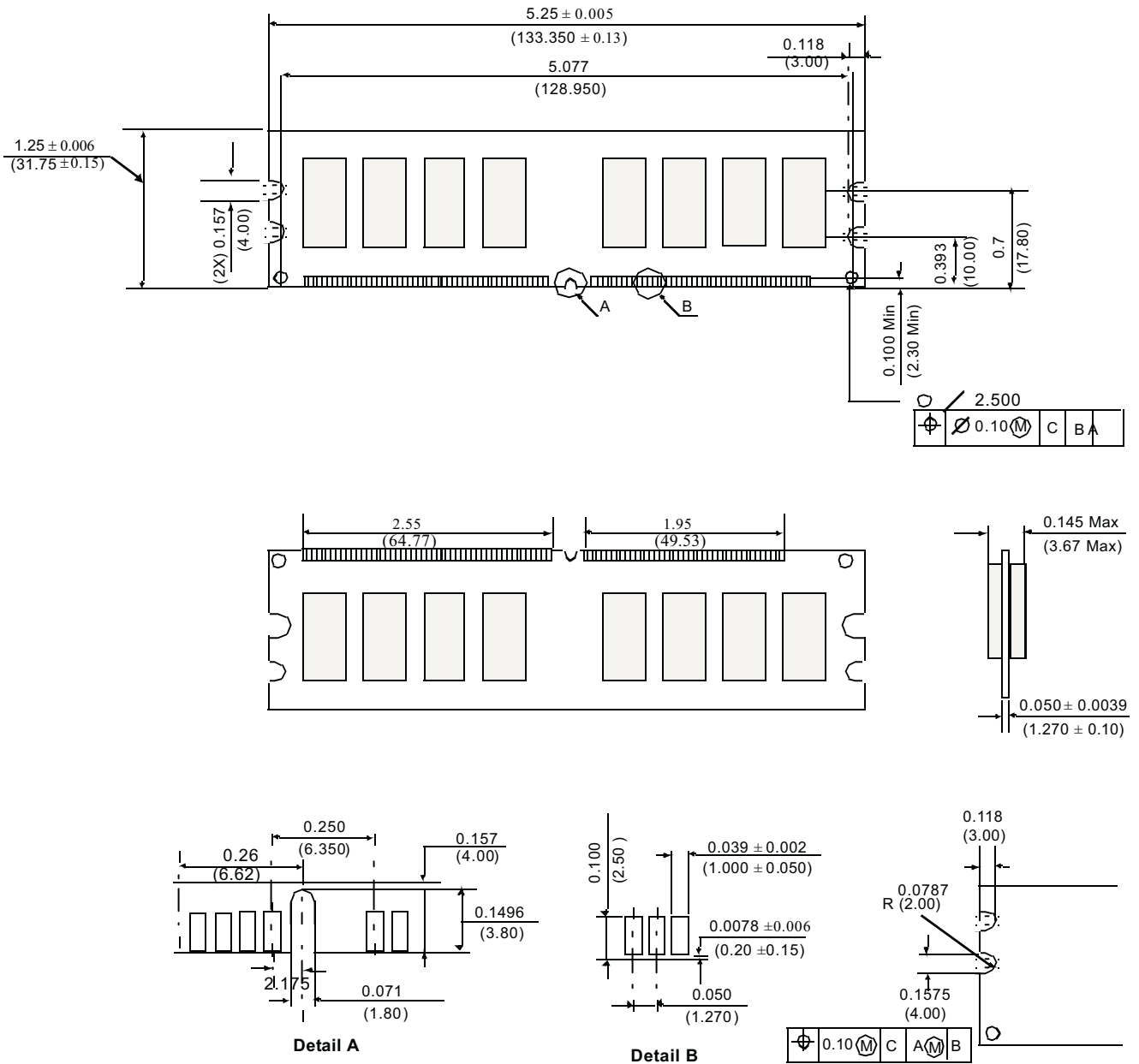
Parameter	Symbol	DDR400 CL3		Unit
		Min	Max	
Row cycle time	tRC	60		ns
Refresh row cycle time	tRFC	70		ns
Row active time	tRAS	40	70K	ns
RAS to CAS delay	tRCD	18		ns
Row precharge time	tRP	18		ns
Row active to Row active delay	tRRD	10		ns
Write recovery time	tWR	15		ns
Internal write to read command delay	tWTR	2		tCK
Clock cycle time	tCK	5	10	ns
Clock high level width	tCH	0.45	0.55	tCK
Clock low level width	tCL	0.45	0.55	tCK
DQS-out access time from CK/CK	tDQ <sub>SCK</sub>	-0.55	+0.55	ns
Output data access time from CK/CK	tAC	-0.65	+0.65	ns
Data strobe edge to output data edge	tDQS <sub>Q</sub>	-	0.4	ns
Read Preamble	tRPRE	0.9	1.1	tCK
Read Postamble	tRPST	0.4	0.6	tCK
CK to valid DQS-in	tDQ <sub>SS</sub>	0.72	1.28	tCK
Write preamble setup time	tWPRES	0		ps
Write preamble	tWPRE	0.25		tCK
Write postamble	tWPST	0.4	0.6	tCK
DQS falling edge to CK rising-setup time	tDSS	0.2		tCK
DQS falling edge from CK rising-hold time	tDSH	0.2		tCK
DQS-in high level width	tDQ <sub>SH</sub>	0.35		tCK
DQS-in low level width	tDQ <sub>SL</sub>	0.35		tCK
Address and Control Input setup time	tIS	0.6		ns
Address and Control Input hold time	tIH	0.6		ns
Data-out high impedance time from CK/CK	tHZ	-	tAC max	ns
Data-out low impedance time from CK/CK	tLZ	tAC min	tAC max	ns
Mode register set cycle time	tMRD	2		tCK
DQ & DM setup time to DQS, slew rate 0.5V/ns	tDS	0.4		ns
DQ & DM hold time to DQS, slew rate 0.5V/ns	tDH	0.4		ns
DQ & DM input pulse width	tDIPW	1.75		ns
Control & Address input pulse width for each input	tIPW	2.2		ns
Refresh interval time	tREFI	7.8		us
Output DQS valid window	tQH	tHP -tQHS	-	ns
Clock half period	tHP	min tCH/tCL	-	ns

**AC Timing Parameters and Specifications (cont.)**

Parameter	Symbol	DDR400 CL3		Unit
		Min	Max	
Data hold skew factor	tQHS		0.5	ns
Auto Precharge write recovery + precharge time	tDAL	-	-	ns
Exit self refresh to non-READ command	tXSNR	75		ns
Exit self refresh to READ command	tXSRD	200	-	tCK

**PACKAGE DIMENSIONS**

Units : Inches (Millimeters)



Tolerances :  $\pm 0.005$ (.13) unless otherwise specified.