Software Transactional Memory and Conditional Critical Regions

Word-Based Systems

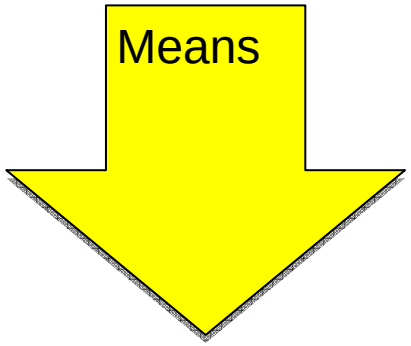
Virginia Tech

Introduction: Motivation

- Language Support for Lightweight Transactions (Harris & Fraser)
- Implement a declarative style of concurrency control where programmers indicate desired safety properties
- New syntax implements Hoare's Conditional Critical Region
- Implemented using their STM

CCR – Conditional Critical Region

```
atomic (condition) {
    statements;
}
```



1. Wait until Condition is satisfied
2. Execute statements atomically

Pattern

```
public int get() {
   atomic (items != 0) {
      items --;
      return buffer[items];
   }
}
```

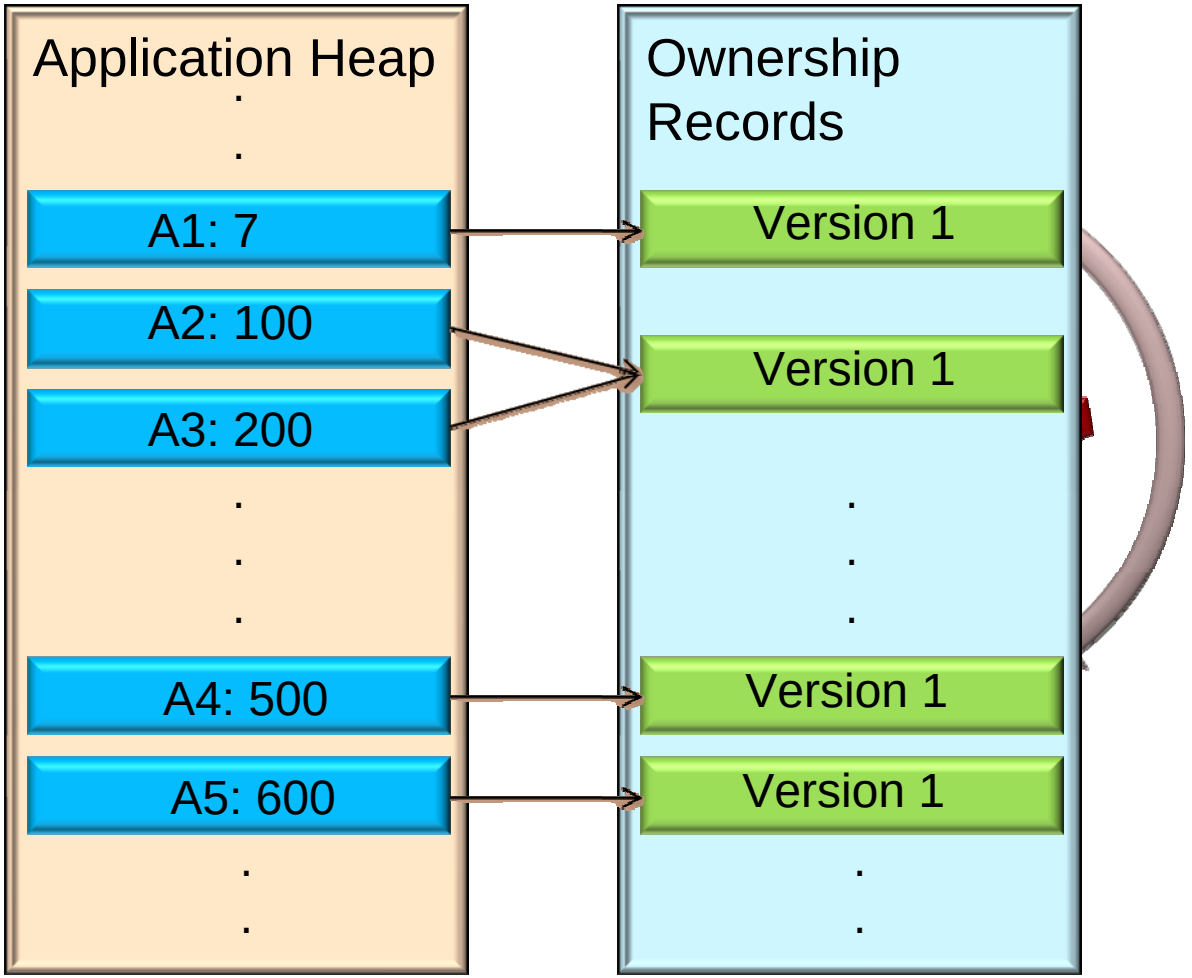
Example Use

CCR Implementation

- Built on top of Software Transactional Memory
- Uses all traditional STM commands and STMWait

```
boolean done = false;
while (!done) {
   STMStart ();
   try {
      if (condition) {
      statements;
      done = STMCommit ();
      } else {
        STMWait();
      }
   } catch (Throwable t) {
      done = STMCommit ();
      if (done) {
         throw t;
      }
   }
}
```

STM Heap Structure



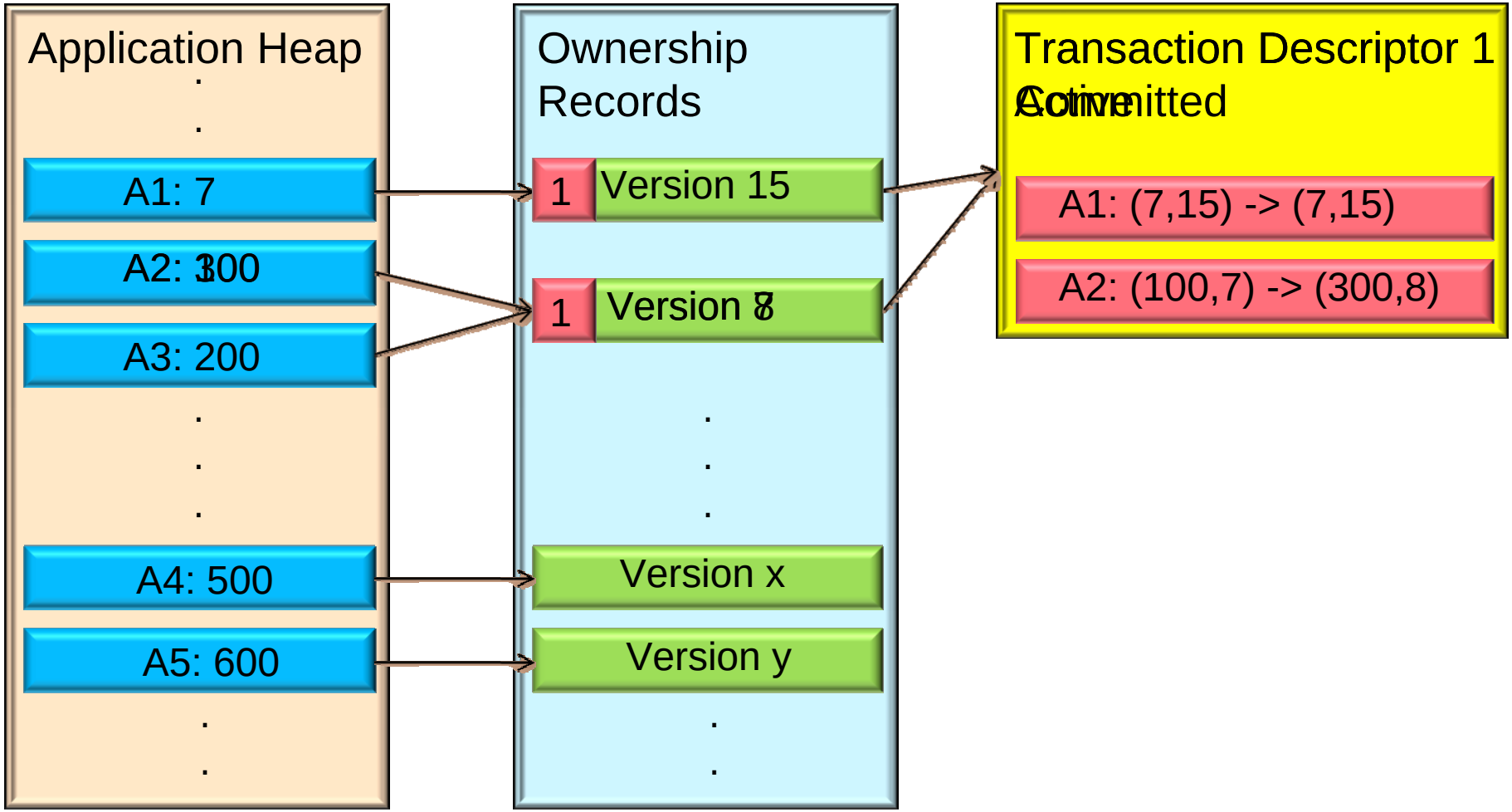
STM - Simple Transaction

```
boolean done = false;
while (true) {
        STMStart();
        readvalues;
        if(STMValidate()){
            statements;
            done = STMCommit();
            if(done) {
               break;
            }
        }
}
```

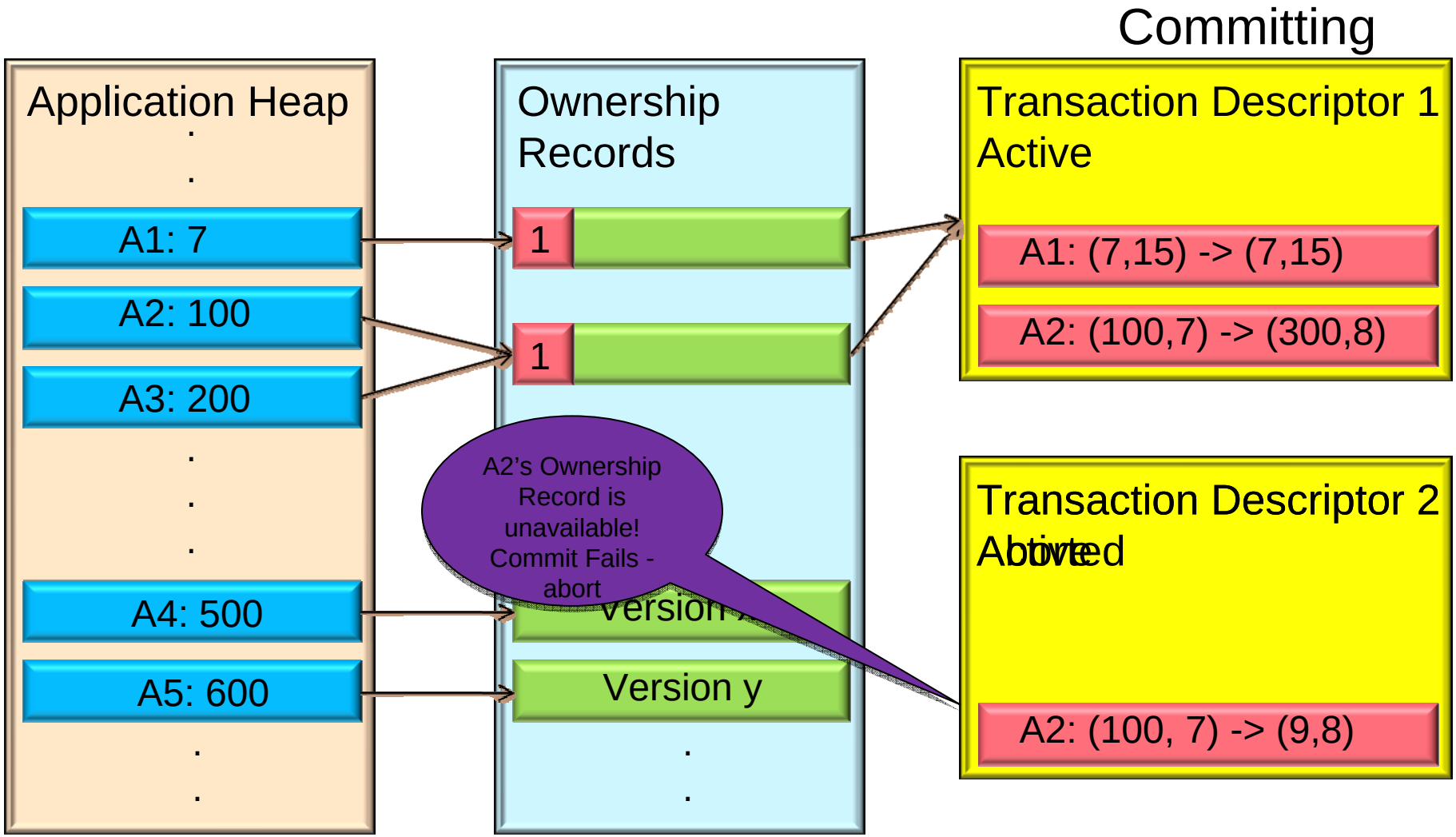
Transaction Management

- STMStart()
- STMAbort()
- STMCommit()
- STMValidate()
- STMWait()

STM - Simple Transaction



STM Collisions - Abort



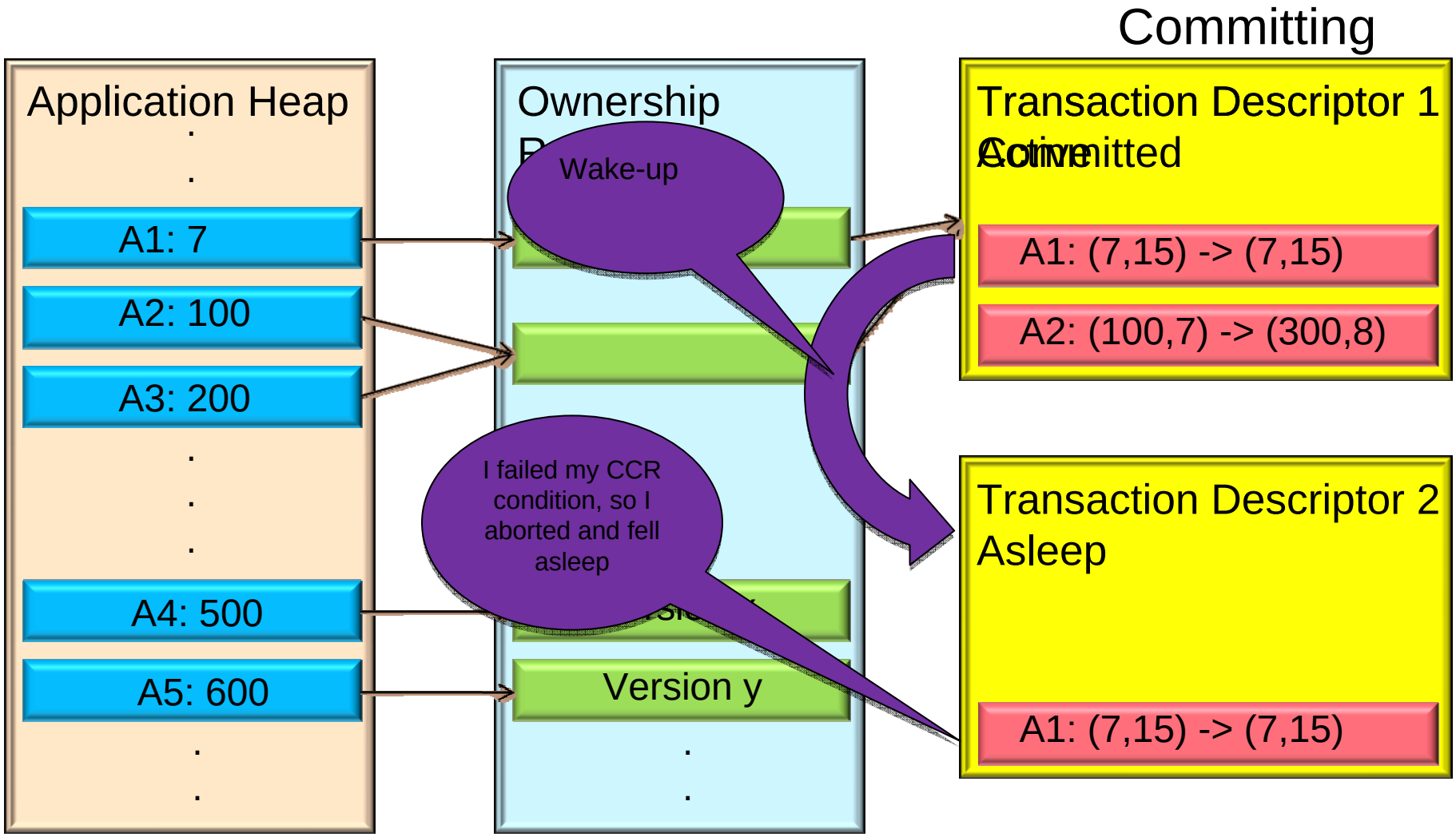
STM Collisions - Sleep

```
atomic (condition) {
    statements;
}
```

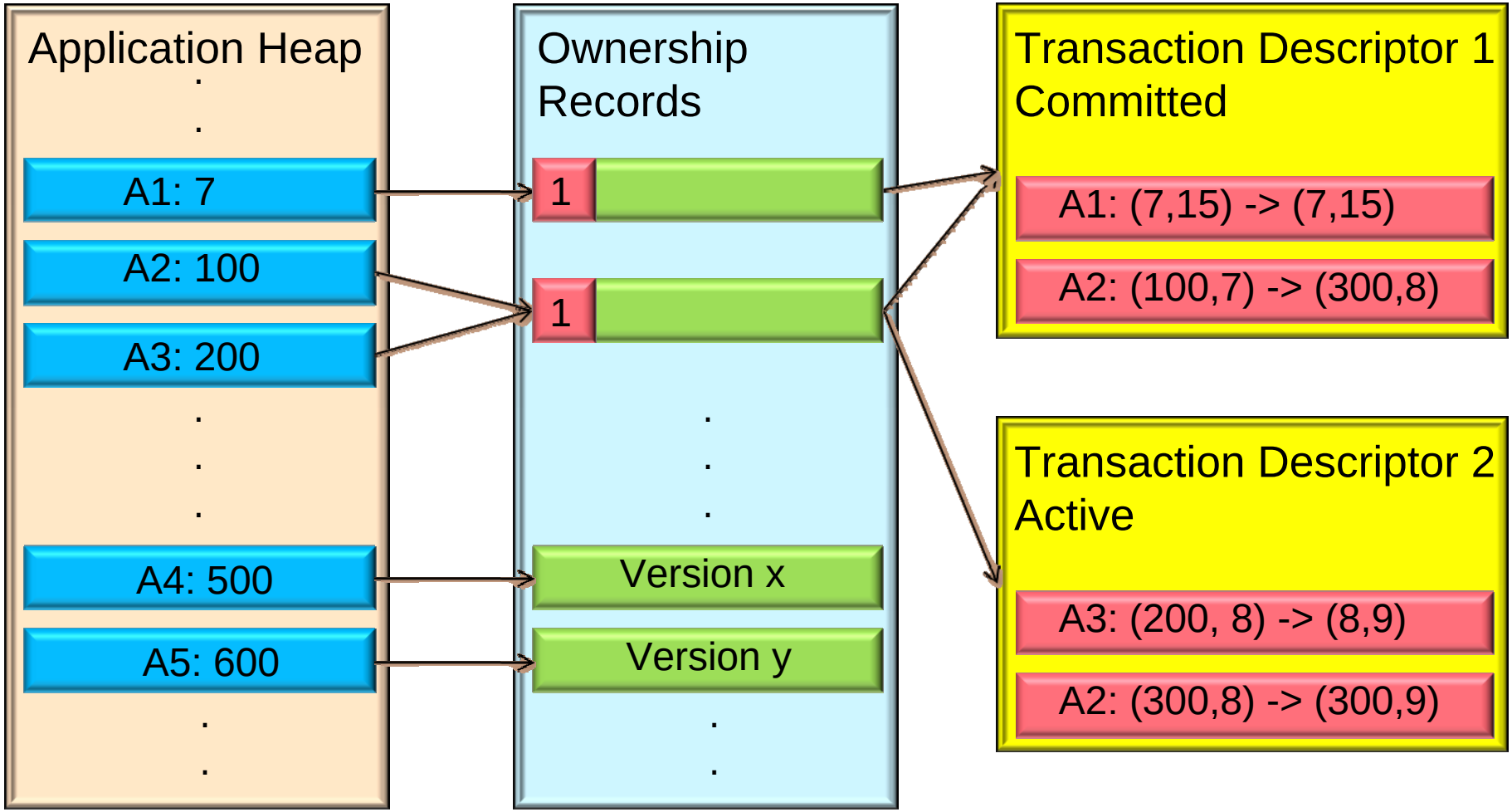
```
boolean done = false;
while (!done) {
   STMStart ();
   try {
      if (condition) {
      statements;
      done = STMCommit ();
      } else {
        STMWait();
      }
   } catch (Throwable t) {
      done = STMCommit ();
      if (done) {
         throw t;
      }
   }
}
```

But when do I wake up?

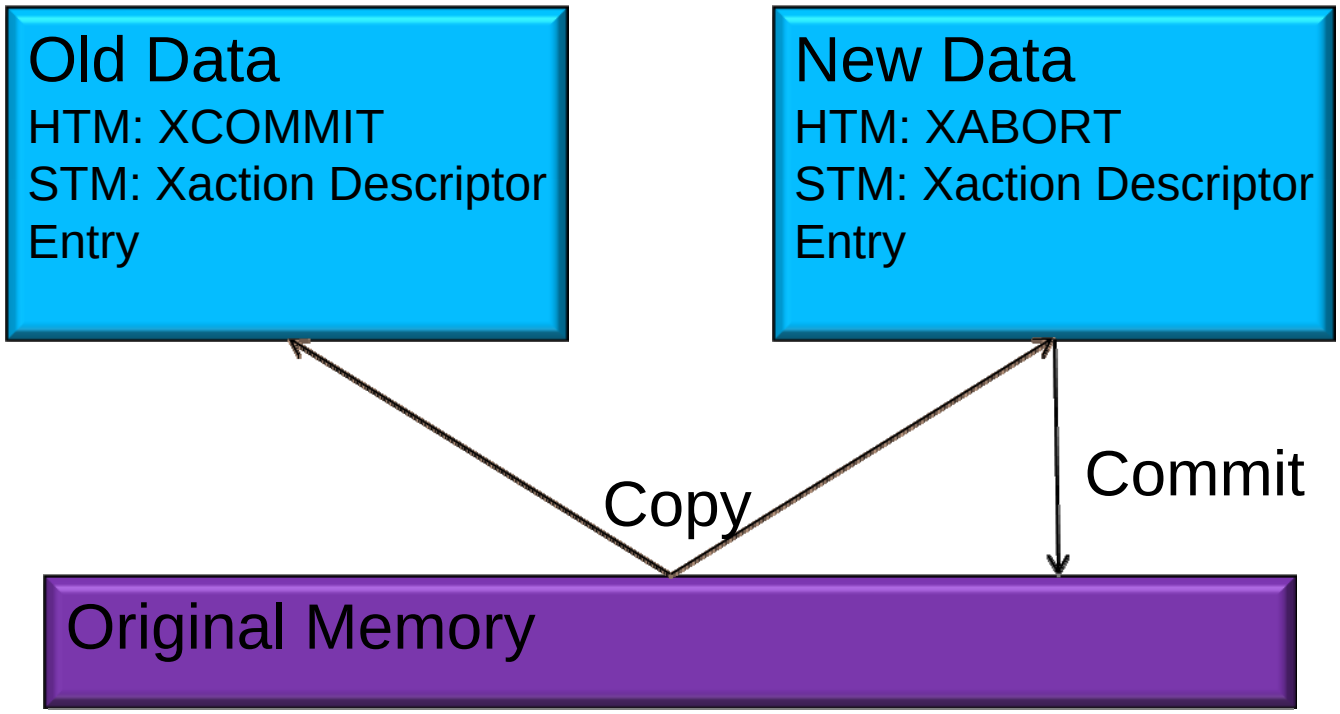
STM Sleep


Committing
Application Heap
A1: 7
A2: 100
A3: 200
A4: 500
A5: 600
Wake-up
I failed my CCR condition, so I aborted and fell asleep
Version y
Transaction Descriptor 1
Committed
A1: (7,15) -> (7,15)
A2: (100,7) -> (300,8)
Transaction Descriptor 2
Asleep
A1: (7,15) -> (7,15)

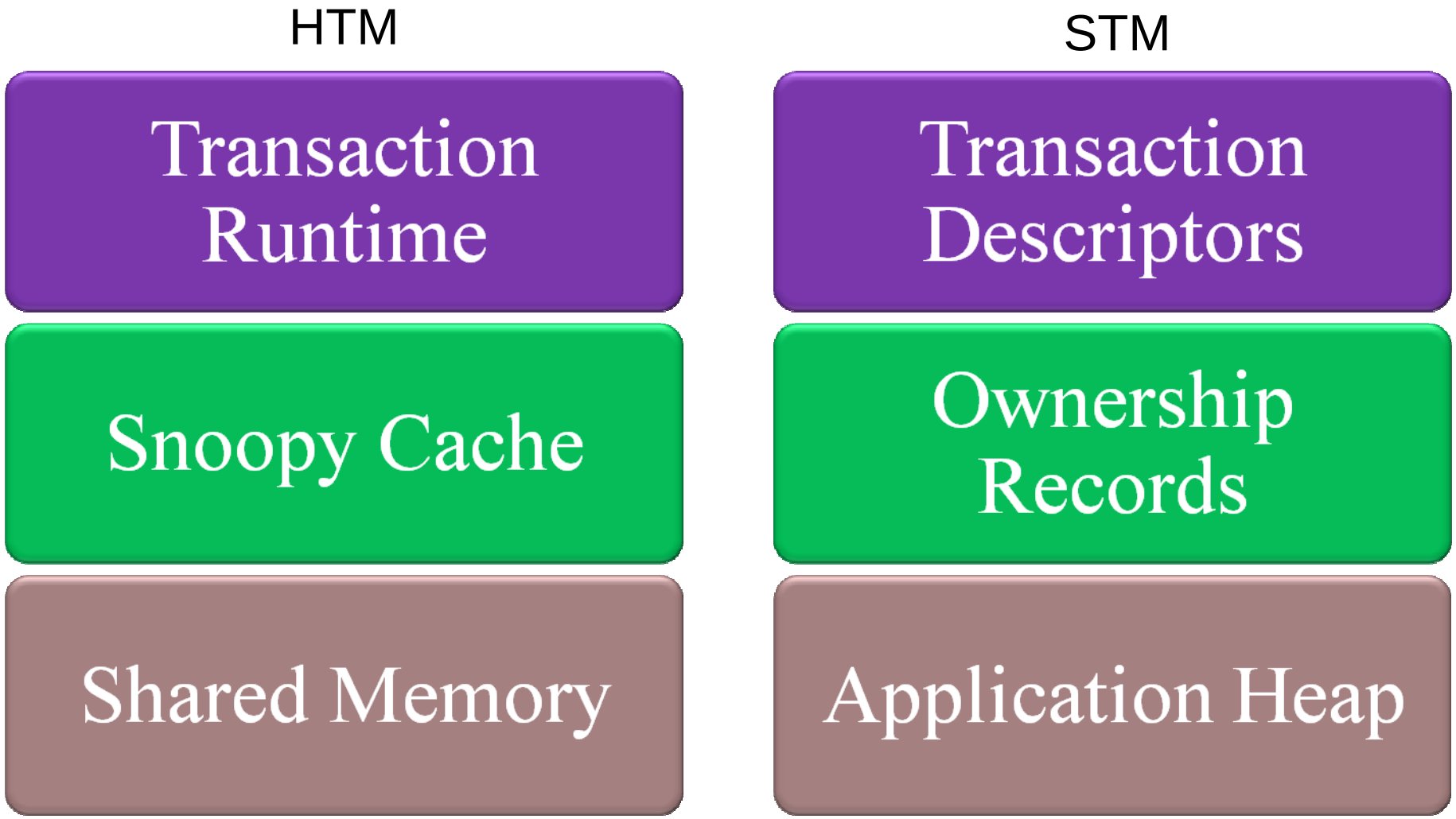
STM Stealing - Optimization



STM – HTM Parallels: Data Copies



STM – HTM Parallels: 3 Tier Implementation



Questions

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