Prepare your answers to the following questions <u>in a plain text file</u>. Submit your file to the Curator system by the posted deadline for this assignment. No late submissions will be accepted. For all questions, show supporting work if you want partial credit.

You will submit your answers to the Curator System (www.cs.vt.edu/curator) under the heading HW07.

For questions 1 through 3, refer to the pipeline design with forwarding, shown below, which supports execution of the following MIPS instructions: add, sub, and, or, slt, lw, sw, and beq. Remember: this pipeline design does not include hazard detection, so it can forward operands but it cannot introduce stalls to deal with situations that forwarding alone will not handle.



1. [20 points] Assume we have the 5-stage pipelined datapath described above, with forwarding hardware but without hazard-detection hardware. Consider executing the following sequence of instructions on this datapath:

| add | \$t5, | \$t2, \$t1 | # | 1.1 |
|-----|-------|------------|---|-----|
| lw | \$t3, | 4(\$t5) | # | 1.2 |
| lw | \$t2, | 0(\$t2) | # | 1.3 |
| or | \$t3, | \$t5, \$t3 | # | 1.4 |
| SW | \$t3, | 0(\$t5) | # | 1.5 |
| | | | | |

You identified all the data hazards present in this sequence of instructions for an earlier assignment. You might want to consult the solution for that assignment before proceeding.

Identify all of the data hazards that can be resolved with forwarding alone (and require forwarding). For each such hazard, state the numbers of the leading and following instructions involved, the register(s) involved, and for each such register, indicate whether the forwarding will be from the EX/MEM interstage buffer or from the MEM/WB interstage buffer.

2. Assume we have the 5-stage pipelined datapath described above, with forwarding hardware but without hazarddetection hardware. Consider executing the following sequence of instructions on this datapath:

| lw | \$t3, | 4(\$t5) | # | 2.1 |
|-----|-------|------------|---|-----|
| add | \$t2, | \$t3, \$t2 | # | 2.2 |
| lw | \$t5, | 0(\$t2) | # | 2.3 |
| add | \$t5, | \$t3, \$t2 | # | 2.4 |
| SW | \$t3, | 0(\$t5) | # | 2.5 |
| or | \$t3, | \$t5, \$t3 | # | 2.6 |

- a) [20 points] Identify all of the data hazards that can be resolved with forwarding alone (and require forwarding). For each such hazard, state the numbers of the leading and following instructions involved, the register(s) involved, and for each such register, indicate whether the forwarding will be from the EX/MEM interstage buffer or from the MEM/WB interstage buffer.
- b) [10 points] Even with forwarding, the given sequence of instructions cannot execute correctly, in the order given without inserting at least one nop instruction. Show how to achieve correct execution by inserting the minimal number of nop instructions, but not reordering the instructions.
- c) [10 points] Can the given sequence of instructions be reordered so that they will execute correctly, using forwarding but without inserting any nop instructions? Justify your answer.
- **3.** Assume we have the 5-stage pipelined datapath described above, with forwarding hardware but without hazard-detection hardware. Consider executing the following sequence of instructions on this datapath:

| \$t3, | 4(\$t4) | # 3.1 |
|-------|---|--|
| \$t2, | \$t1, \$t3 | # 3.2 |
| \$t5, | 0(\$t2) | # 3.3 |
| \$t4, | 0(\$t1) | # 3.4 |
| \$t3, | \$t4, \$t5 | # 3.5 |
| | \$t3, \$t2, \$t5, \$t4, \$t3, | <pre>\$t3, 4(\$t4) \$t2, \$t1, \$t3 \$t5, 0(\$t2) \$t4, 0(\$t1) \$t3, \$t4, \$t5</pre> |

- a) [15 points] Identify all of the data hazards that <u>cannot</u> be resolved with forwarding. For each such hazard, state the numbers of the leading and following instructions involved, the register(s) involved, and for each such register, indicate whether the forwarding will be from the EX/MEM interstage buffer or from the MEM/WB interstage buffer.
- b) [15 points] Can the given sequence of instructions be reordered so that they will execute correctly, using forwarding but without inserting any nop instructions? Justify your answer.