Questions 1 through 4 refer to the completed single-cycle datapath design, reproduced below, which supports execution of the following MIPS instructions: add, sub, and, or, slt, lw, sw, beq and j.

1. Suppose that, due to a manufacturing defect, the AND gate suffers a stuck-at-1 error. That is, the output from the AND gate is always set to 1 regardless of circumstances. Assume that the rest of the hardware operates as designed.
   a) [12 points] Would any of the supported instructions still always execute correctly? If so, which one(s) and why?
   b) [12 points] Would any of the other supported instructions possibly execute correctly (i.e., produce all the logically correct results and not produce any unintended side effects)? If so, which one(s) and why?

2. Suppose that, due to a manufacturing defect, the Zero control signal suffers a stuck-at-0 error. That is, the Zero line is always set to 0 regardless of circumstances. Assume that the rest of the hardware operates as designed.
   a) [12 points] Would any of the supported instructions still always execute correctly? If so, which one(s) and why?
   b) [12 points] Would any of the other supported instructions possibly execute correctly (i.e., produce all the logically correct results and not produce any unintended side effects)? If so, which one(s) and why?
3. The Data Memory unit has a control signal MemRead that can be used to prevent read operations. But there is no provision in this design for preventing the Register unit from performing read operations. In fact, the Register unit will always read from two registers no matter which instruction is being executed.

Obviously, the design could have included a RegRead signal as well as the existing RegWrite signal, so this omission appears be a deliberate decision.

a) [12 points] Give an example of a supported assembly instruction whose execution would be expected to have undesired consequences if the MemRead signal was not used to prevent a memory read. Hint: don't forget that there will be an operating system in play, not just the hardware shown in the diagram. Explain your example carefully.

b) [12 points] Explain why the issue you illustrated in the first part of this question cannot arise when a register is read.

4. A few easy ones... aside from the first part, no explanations are necessary.

a) [7 points] The value 4 is added to the value from the PC register. Why is the value 4 used?

b) [7 points] How many bits wide is the line that goes from Read data 2 to Write data?

c) [7 points] Assuming all the other control signals are set as usual, which of the supported instructions will always execute correctly if the MemtoReg control signal suffered a stuck-at-0 error?

d) [7 points] Assuming all the other control signals are set as usual, which of the supported instructions will always execute correctly if the RegDst control signal suffered a stuck-at-1 error?