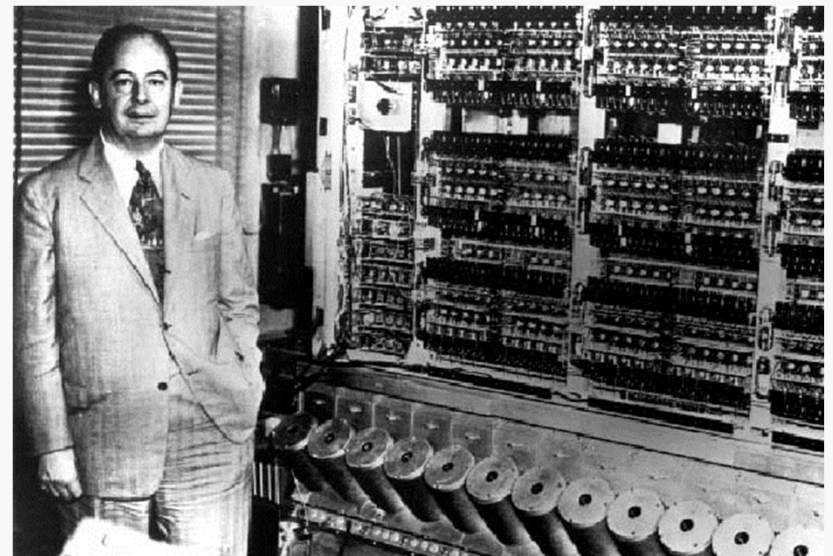


1945: John von Neumann

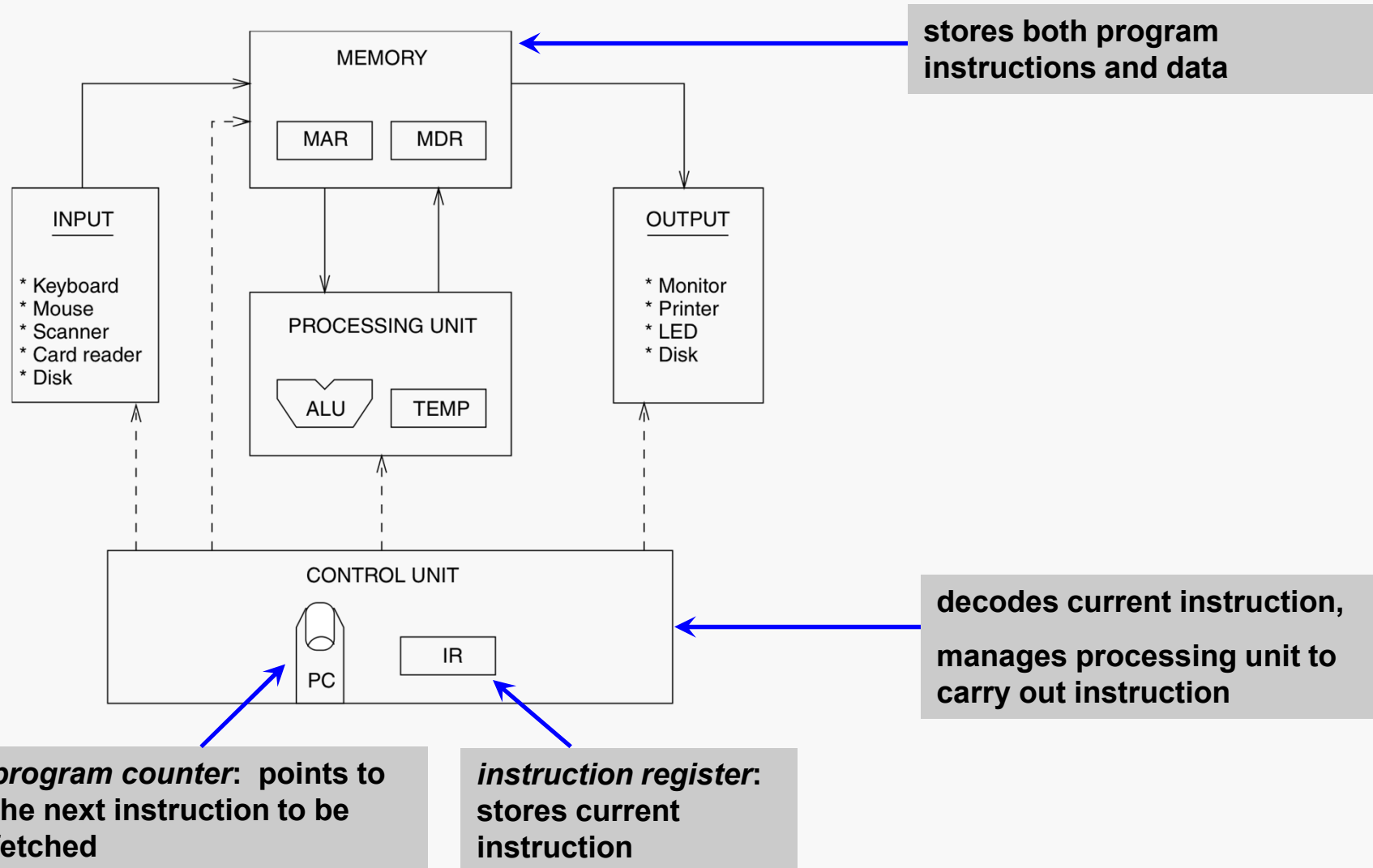
- Wrote a report on the stored program concept, known as the First Draft of a Report on EDVAC
- also Alan Turing... Konrad Zuse... Eckert & Mauchly...

The basic structure proposed in the draft became known as the “von Neumann machine” (or model).

- a memory, containing instructions and data
- a processing unit, for performing arithmetic and logical operations
- a control unit, for interpreting instructions



## Abstraction of von Neumann Architecture



Totally dominate laptop/desktop/server market

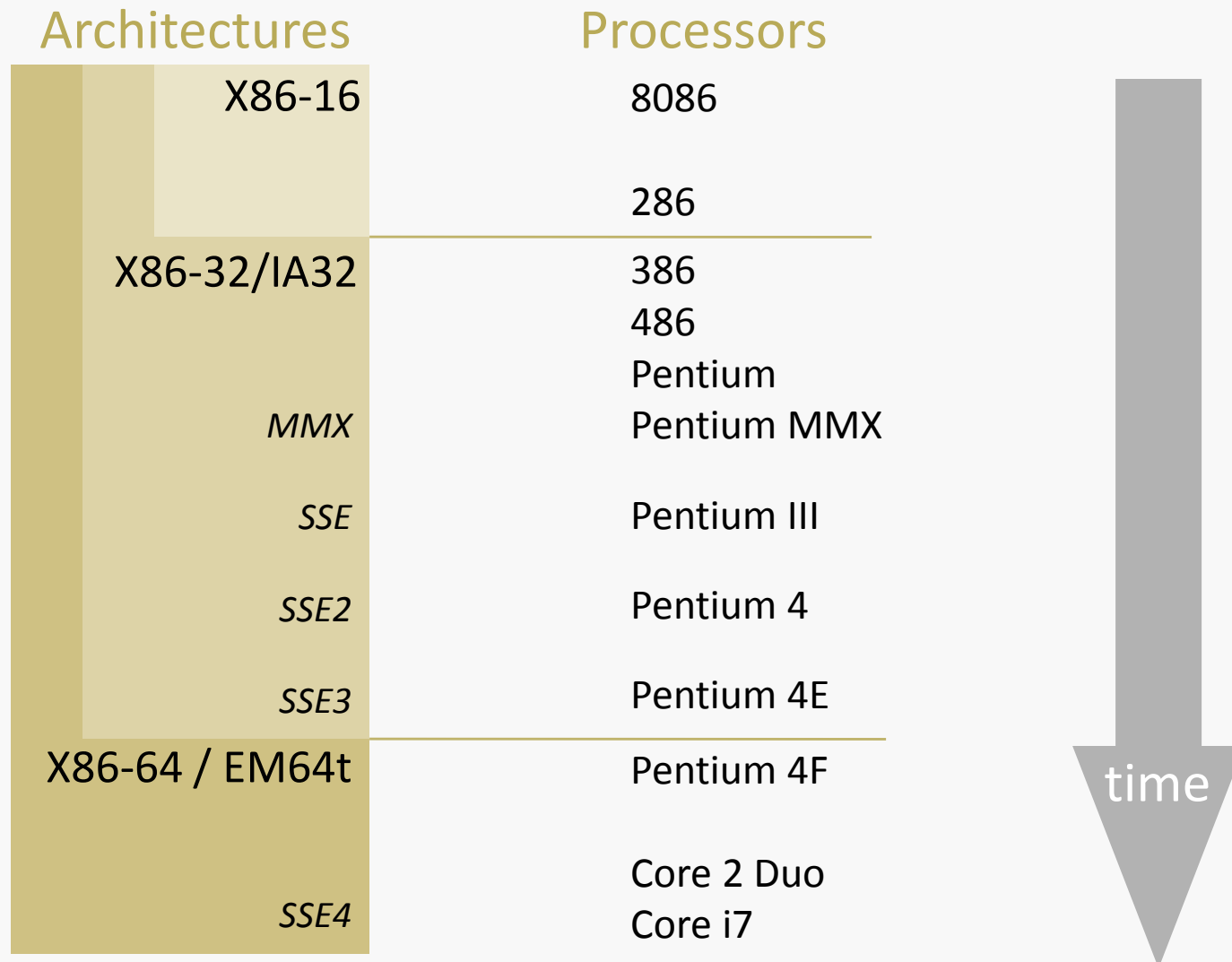
Evolutionary design

- Backwards compatible up until 8086, introduced in 1978
- Added more features as time goes on

Complex instruction set computer (CISC)

- Many different instructions with many different formats
  - But, only small subset encountered with Linux programs
- Hard to match performance of Reduced Instruction Set Computers (RISC)
- But, Intel has done just that!
  - In terms of speed. Less so for low power.

<i>Name</i>	<i>Date</i>	<i>Transistors</i>	<i>MHz</i>
8086	1978	29K	5-10
<ul style="list-style-type: none"><li>– First 16-bit processor. Basis for IBM PC &amp; DOS</li><li>– 1MB address space</li></ul>			
80386	1985	275K	16-33
<ul style="list-style-type: none"><li>– First 32 bit processor , referred to as IA32</li><li>– Added “flat addressing”</li><li>– Capable of running Unix</li><li>– 32-bit Linux/gcc uses no instructions introduced in later models</li></ul>			
Pentium 4F	2004	125M	2800-3800
<ul style="list-style-type: none"><li>– First 64-bit processor, referred to as x86-64</li></ul>			
Core i7	2008	731M	2667-3333
<ul style="list-style-type: none"><li>– Our shark machines</li></ul>			



## Intel Attempted Radical Shift from IA32 to IA64

- Totally different architecture (Itanium)
- Executes IA32 code only as legacy
- Performance disappointing

## AMD Stepped in with Evolutionary Solution

- x86-64 (now called “AMD64”)

## Intel Felt Obligated to Focus on IA64

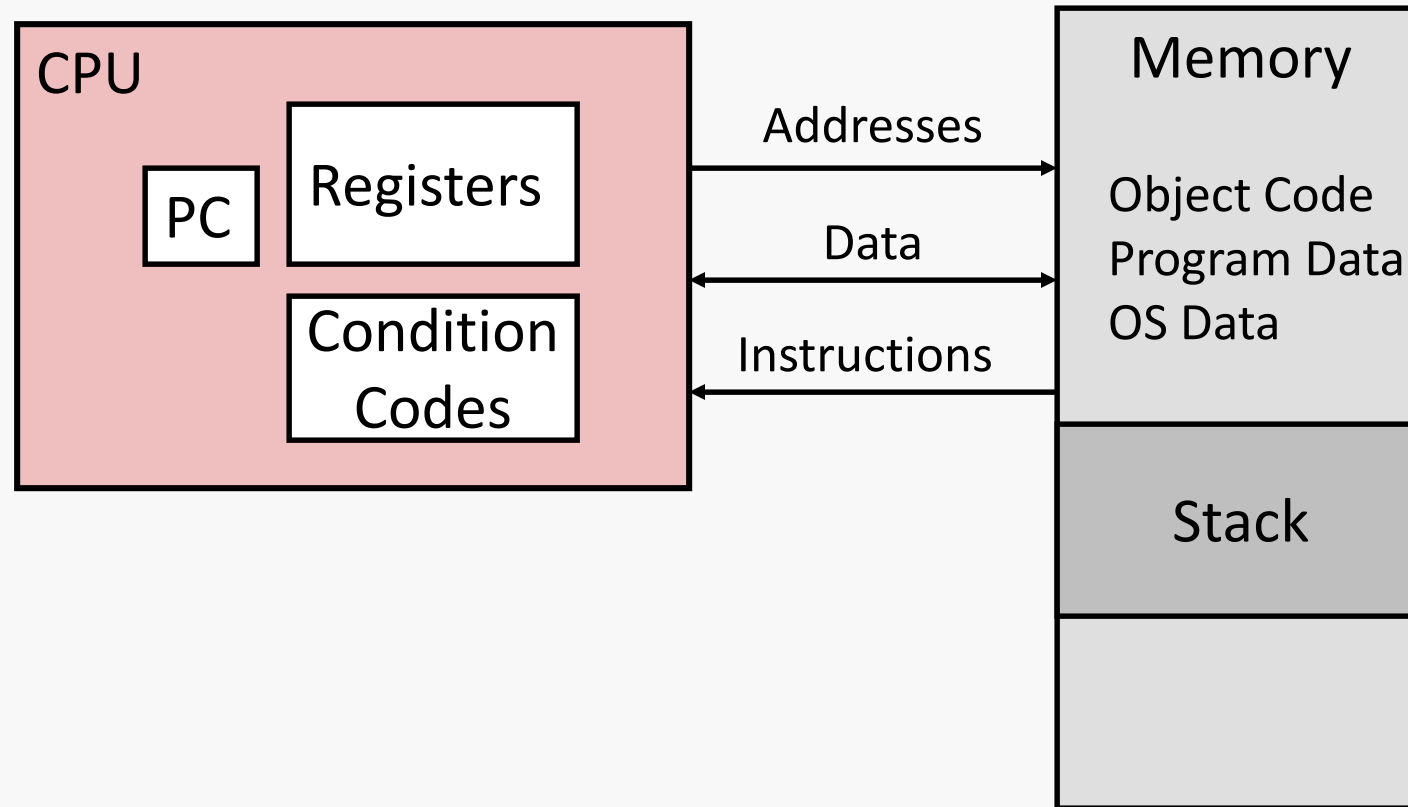
- Hard to admit mistake or that AMD's approach is better

## 2004: Intel Announces EM64T extension to IA32

- Extended Memory 64-bit Technology
- Almost identical to x86-64!

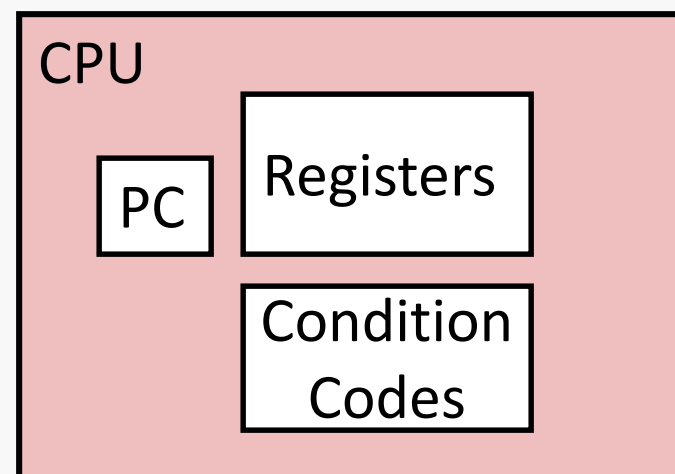
## All but low-end x86 processors support x86-64

- But, lots of code still runs in 32-bit mode

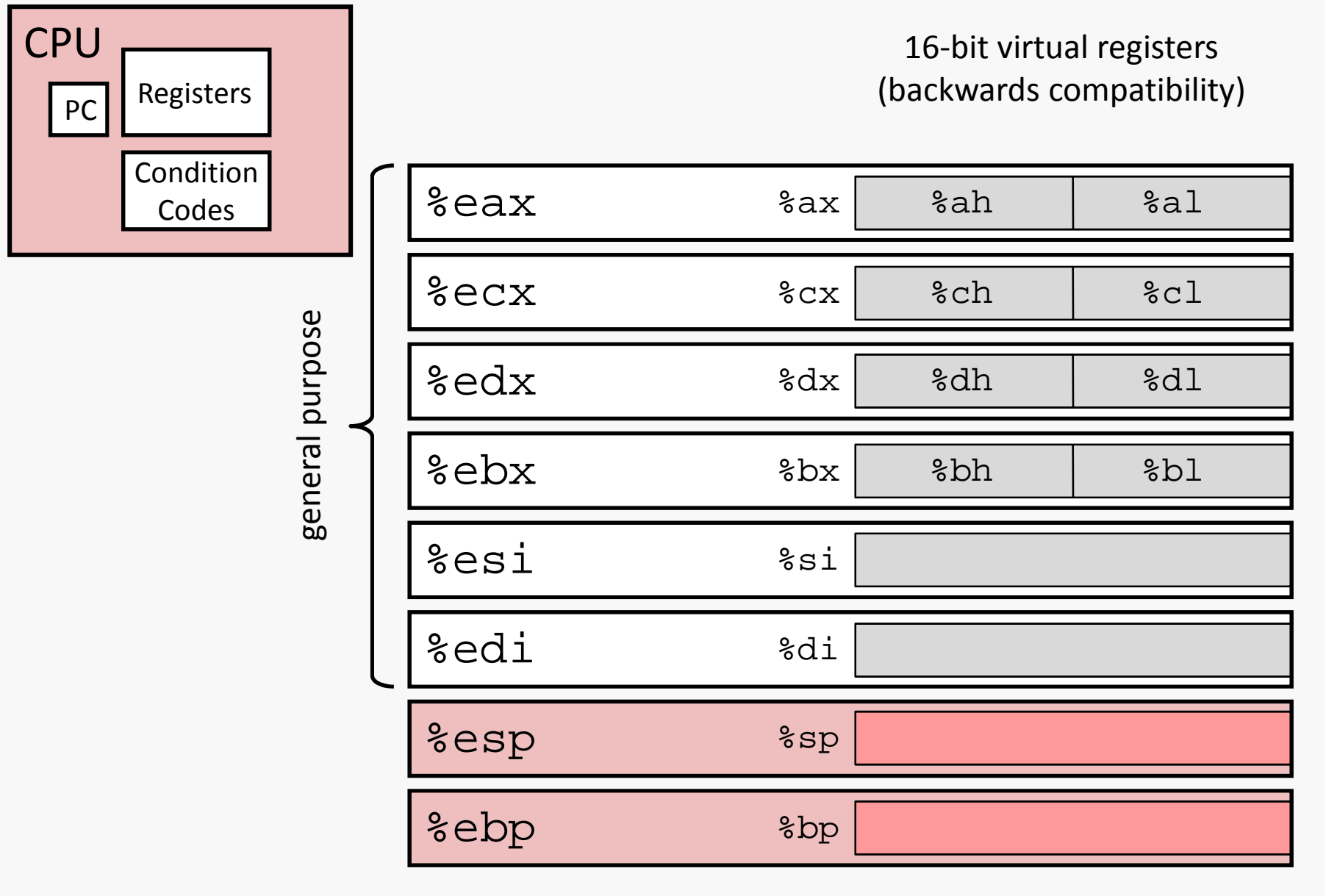


## Programmer-Visible State

- PC: Program counter
  - Address of next instruction
  - Called “EIP” (IA32) or “RIP” (x86-64)
- Register file
  - Heavily used program data
- Condition codes
  - Store status information about most recent arithmetic operation
  - Used for conditional branching

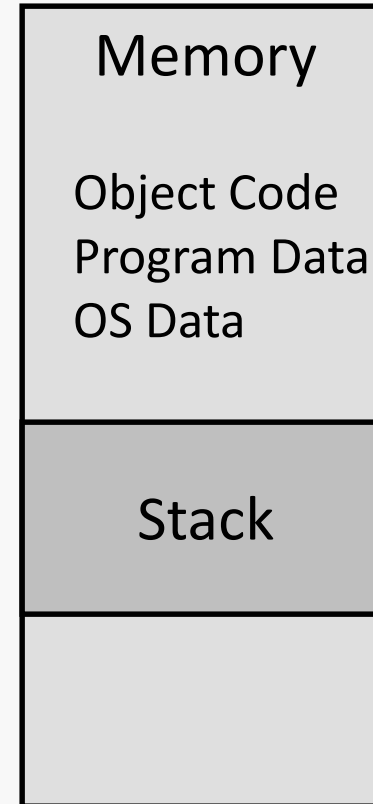






## – **Memory**

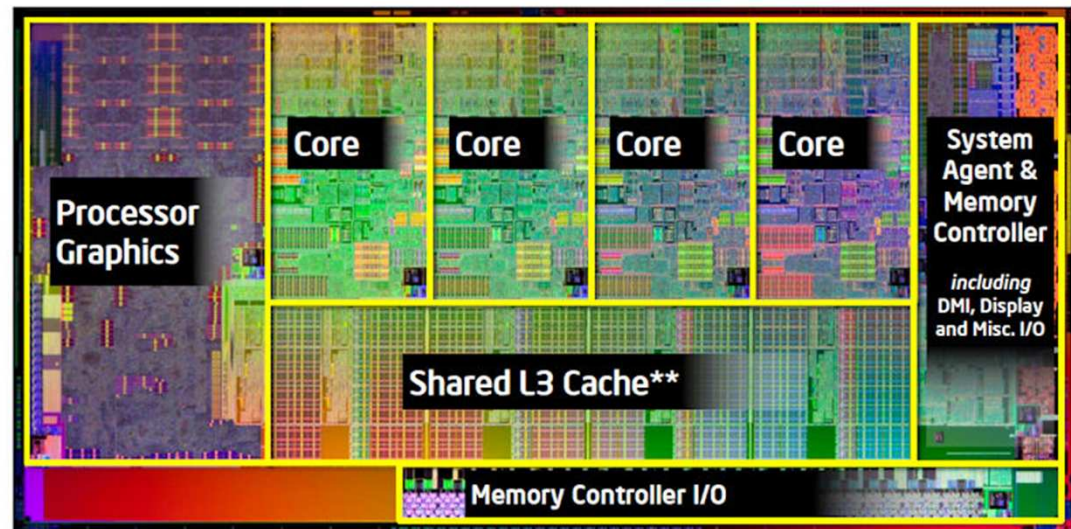
- Byte addressable array
- Code, user data, (some) OS data
- Includes stack used to support procedures



```
// C code
. . .
int imax(int first, int second) {

    if ( first >= second )
        return first;
    return second;
}
```

But the hardware only  
"understands" binary  
representations



```
int imax(int first, int second) {  
    if ( first >= second )  
        return first;  
    return second;  
}
```

`gcc -O0 -c -m32 -std=c99imax.c`



```
457f464c010100010000000000000000  
00010003000100000000000000000000  
00bc000000000000000003400000000028  
0009000689558be50845453b7c0c8b05  
084503eb458b5d0c00c3000047004343  
203a55287562746e2f75694c616e6f72  
3420352e322e382d62756e7575742934  
.  
.  
.
```

But who wants to  
program in binary?

```
int imax(int first, int second) {  
    if ( first >= second )  
        return first;  
    return second;  
}
```

**Solution:**

translate high-level language code  
into intermediate-level code which is  
more human-friendly,  
then translate that "assembly" code  
into the machine's language.

```
. . .  
imax:  
    pushl    %ebp  
    movl     %esp, %ebp  
  
    movl     8(%ebp), %eax  
    cmpl     12(%ebp), %eax  
    jl       .L2  
    movl     8(%ebp), %eax  
    jmp      .L3  
  
.L2:  
    movl     12(%ebp), %eax  
  
.L3:  
    popl     %ebp  
    ret  
  
. . .
```

	Source	Dest	Src, Dest	C Analog
movl	Imm	Reg	movl \$0x4, %eax	tmp = 0x4;
		Mem	movl \$-147, (%eax)	*p = -147;
	Reg	Reg	movl %eax, %edx	tmp2 = tmp1;
		Mem	movl %eax, (%edx)	*p = tmp;
	Mem	Reg	movl (%eax), %edx	tmp = *p;

<b>%rax</b>	<b>%eax</b>
<b>%rbx</b>	<b>%ebx</b>
<b>%rcx</b>	<b>%ecx</b>
<b>%rdx</b>	<b>%edx</b>
<b>%rsi</b>	<b>%esi</b>
<b>%rdi</b>	<b>%edi</b>
<b>%rsp</b>	<b>%esp</b>
<b>%rbp</b>	<b>%ebp</b>

<b>%r8</b>	<b>%r8d</b>
<b>%r9</b>	<b>%r9d</b>
<b>%r10</b>	<b>%r10d</b>
<b>%r11</b>	<b>%r11d</b>
<b>%r12</b>	<b>%r12d</b>
<b>%r13</b>	<b>%r13d</b>
<b>%r14</b>	<b>%r14d</b>
<b>%r15</b>	<b>%r15d</b>

- Extend existing registers. Add 8 new ones.
- Make **%ebp/%rbp** general purpose

```
int imax(int first, int second) {  
    if ( first >= second )  
        return first;  
    return second;  
}
```

```
. . .  
    movl    %edi, -4(%rbp)  
    movl    %esi, -8(%rbp)  
    movl    -4(%rbp), %eax  
    cmpl    -8(%rbp), %eax  
    jl      .L2  
    movl    -4(%rbp), %eax  
    jmp     .L3  
.L2:  
    movl    -8(%rbp), %eax  
.L3:  
. . .
```